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SECTION 1

INTRODUCTION

1.1 OVERVIEW

This technical reference data provides the information necessary to perform installation, preventive maintenance, calibration, and corrective maintenance (troubleshooting) on a UniPak 2B installed in a Data I/O Universal Programmer (29B, 29A, Series 19, or Model 100A). Instructions on how to operate the UniPak 2B are not included in this manual. Refer to the UniPak 2B Operator's Manual (part number 981-0179) for operating instructions.

The manual is broken into six sections and two appendices. The following subsections contain a synopsis of each section, beginning with Section 2.

1.2 UNIPAK 2B INSTALLATION

Section 2 (Installation) provides instructions on how to install and remove the UniPak 2B from the Universal Programmer and how to install and remove the Pinout Cartridge from the UniPak 2B. It also includes repackaging information if the UniPak 2B must be returned for service.

1.3 CIRCUIT DESCRIPTION

Section 3 (Circuit Description) gives a two level block diagram description of the UniPak 2B opertation. The highest level diagrams the instrument by (printed circuit) boards. This is followed by a detailed block diagram of the individual boards in the instrument.

1.4 MAINTENANCE

Section 4 (Maintenance) provides information on the assembly and disassembly of the UniPak 2B. It also provides cleaning and preventive maintenance instructions.

1.5 CALIBRATION

Section 5 (Calibration) gives the calibration instructions for the UniPak 2B.

1.6 TROUBLESHOOTING

Section 6 (Troubleshooting) contains corrective maintenance instructions for the UniPak 2B. It also contains procedures to isolate the problem to the UniPak 2B or the Universal Programmer.

1.7 FAMILY/PINOUT CODES

Appendix A (Family/Pinout Codes) contains a list of the applicable Data I/O Family Codes, Pinout Codes, Pinout Cartridge model number, software version, and approval status.

1.8 SCHEMATICS

Appendix B (Schematics) contains the schematics of the printed circuit boards installed in the UniPak 2B and the pinout cartridges available.

SECTION 2

INSTALLATION

2.1 INSPECTION

Your UniPak 2B was tested both electrically and mechanically before it was shipped, and was carefully packaged to prevent shipping damage. It should, therefore, arrive free of any defect, without marks or scratches, and in perfect operating condition. However, carefully inspect the instrument for any damage that may have occurred in transit. If you note any damage, file a claim with the carrier and notify Data I/O.

2.2 UNIPAK 2B INSTALLATION

The UniPak 2B may be installed and removed with the programmer's power on; this feature allows you to retain data in RAM during module changes. If the programmer power is turned on before the UniPak 2B is installed, you will hear a beep until the UniPak 2B is installed.

CAUTION

To prevent device damage from voltage transients be sure that all sockets are empty before you:

- o switch programmer power on or off
- o install or remove the UniPak 2B

Use the following procedure to install the UniPak 2B:

1. Slide the UniPak 2B into the opening in the programmer (figure 2-1).
2. Tilt the UniPak 2B up and gently push it back to hook the flange of the UniPak 2B over the back edge of the programmer opening (figure 2-1a).
3. Lower the UniPak 2B into position as shown in figure 2-1b.
4. Press gently on the front edge of the UniPak 2B to ensure a good connection (figure 2-1c).

2.3 UNIPAK 2B REMOVAL

Use the following procedure to remove the UniPak 2B:

1. Make sure the programmer has completed all operations, i.e., if the action symbol is on the display wait until the operation is complete (the action symbol disappears).

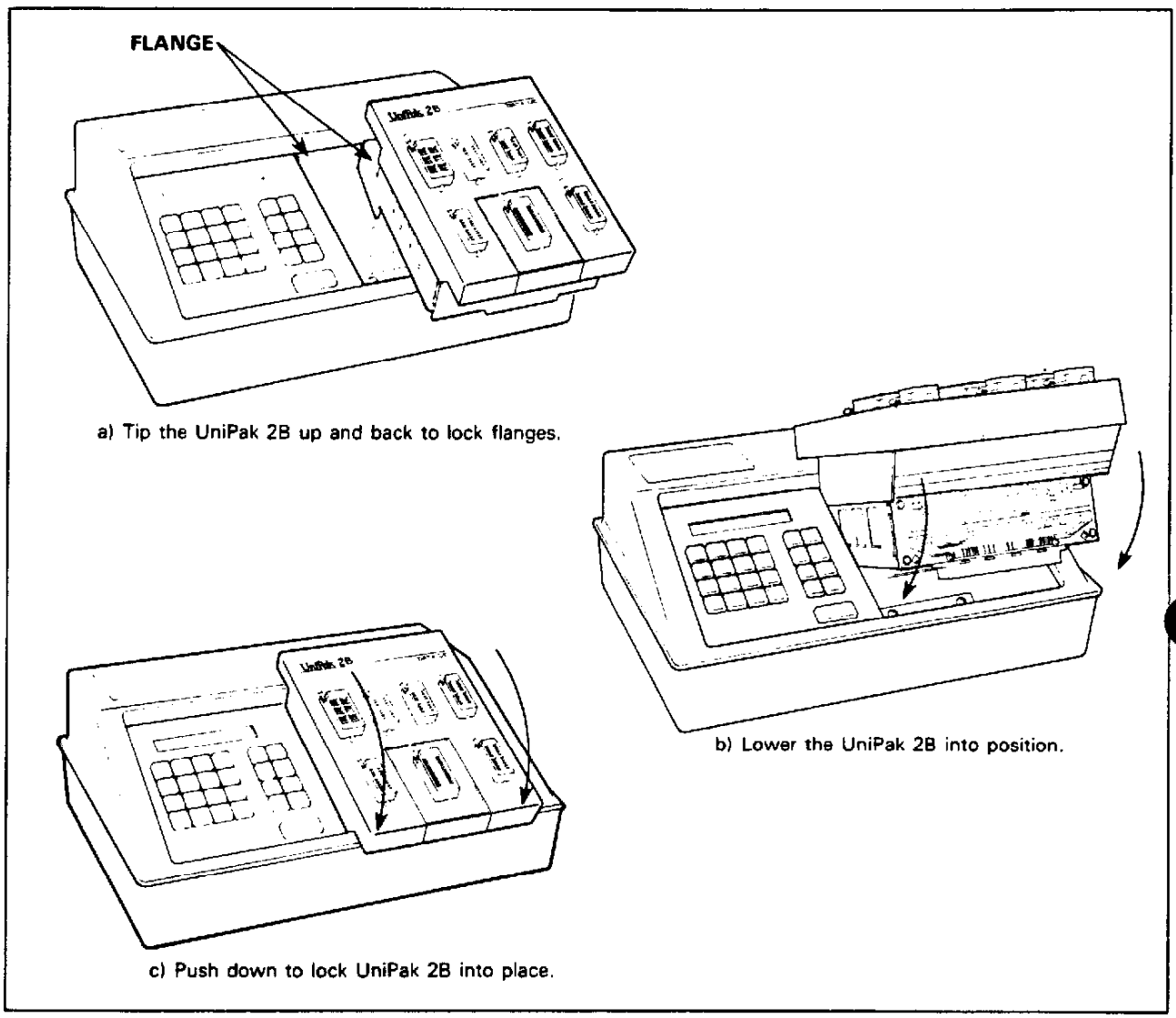


Figure 2-1. UniPak 2B Installation

2. Make sure any device(s) is removed from the socket(s). (Refer to the programmer manual for instructions, if required.)

3. Tilt the UniPak 2B up and gently remove it from the programmer.

2.4 PINOUT CARTRIDGE REMOVAL

One socket (number 6) on the UniPak 2B is removable so that any one of a series of pinout cartridges can be installed in that position. This allows the UniPak 2B more flexibility in programming non-standard devices.

Use the following procedure to remove an installed pinout cartridge from the UniPak 2B:

1. Remove power from the universal programmer in which the UniPak 2B is installed.

CAUTION

If it is impractical to remove power from the programmer because of data loaded in RAM remove the UniPak 2B from the programmer and then remove the pinout cartridge from the UniPak 2B.

2. Steady the UniPak 2B with one hand while curling the fingers of the other hand around the lip on the bottom rear of the pinout cartridge and pressing the thumb against the frame of the UniPak 2B. Apply pressure with the hand on the pinout cartridge until the card edge connector comes free from the UniPak 2B connector.

3. Slide the pinout cartridge to the rear until it is clear of the UniPak 2B pinout cartridge opening, then lift the pinout cartridge clear of the UniPak 2B.

2.5 PINOUT CARTRIDGE INSTALLATION

Use the following procedure to install a pinout cartridge in the UniPak 2B:

1. Remove power from the universal programmer in which the UniPak 2B is installed.

CAUTION

If it is impractical to remove power from the programmer because of data loaded in RAM remove the UniPak 2B from the programmer and then install the pinout cartridge in the UniPak 2B.

2. Place the front one-third of the pinout cartridge on the guides in the opening for socket #6.

3. Slide the pinout cartridge forward until the card-edge connector on the front of the module comes in contact with the connecter on the UniPak 2B. The lip on each side of the UniPak 2B opening should slide into the channel on each side of the pinout cartridge.

4. Steady the UniPak 2B with one hand and push against the rear of the pinout cartridge with the other until it snaps in place in the UniPak 2B connector.

5. The pinout cartridge is now ready to use.

2.6 REPACKING FOR SHIPMENT

If the UniPak 2B is to be shipped to Data I/O for service or repair, attach a tag to it describing the work required and identifying the owner. In correspondence, identify the unit by part number, revision level, and name. If the original shipping container is to be used, place the UniPak 2B in the container with the appropriate packing material and seal the container with strong tape. If another container is used, be sure that it is a heavy carton, wrapped with heavy paper or plastic; use appropriate packing material and seal well with strong tape. Mark the container "DELICATE INSTRUMENT" or "FRAGILE."

SECTION 3

CIRCUIT DESCRIPTION

3.1 OVERVIEW

This section defines the functions of UniPak 2B principal hardware components. Each circuit-card assembly is depicted by a block diagram accompanied by a written description.

3.2 GENERAL ARCHITECTURE

Data is input to the UniPak 2B through the Universal Programmer's bus. The resultant commands are processed in the UniPak 2B and output to the sockets on the UniPak 2B's address, data, and control buses. Each of these operations are described below.

3.2.1 LINK BETWEEN THE UNIPAK 2B AND PROGRAMMER

The UniPak 2B is controlled by the programmer's extended processor bus through the UniPak 2B mating connector (J1). The control software for the UniPak 2B is located in EPROM on the memory card (702-1650).

3.2.2 THE BUSES

The programmer's address bus, data bus, R/$\overline{W}$ line, and $\overline{V \cdot 0_2}$ line access the software on the memory card and control the gates and registers on the waveform generator (701-1690) and address cards (701-1655). The UniPak 2B's device bus gathers the programming waveforms produced by these cards and transmits them to the socket card (701-0153). Figure 3-1 shows the relationships between the buses.

3.3 COMPONENT LAYOUT

The principal components of the UniPak 2B are the motherboard, the waveform generator, the address card, the memory card, the socket card, and the interchangeable pinout cartridge. The component layout of the UniPak 2B is shown in figure 3-2 and described in the following subsections.

3.3.1 MOTHERBOARD

The motherboard accepts on J1 the signals and power supplies from J6 of the programmer, and transmits them to two identical 72-pin edge connectors (J2 and J3) and a 50-pin edge connector (P1). (Refer to figure 3-3 and schematic 30-702-1661).

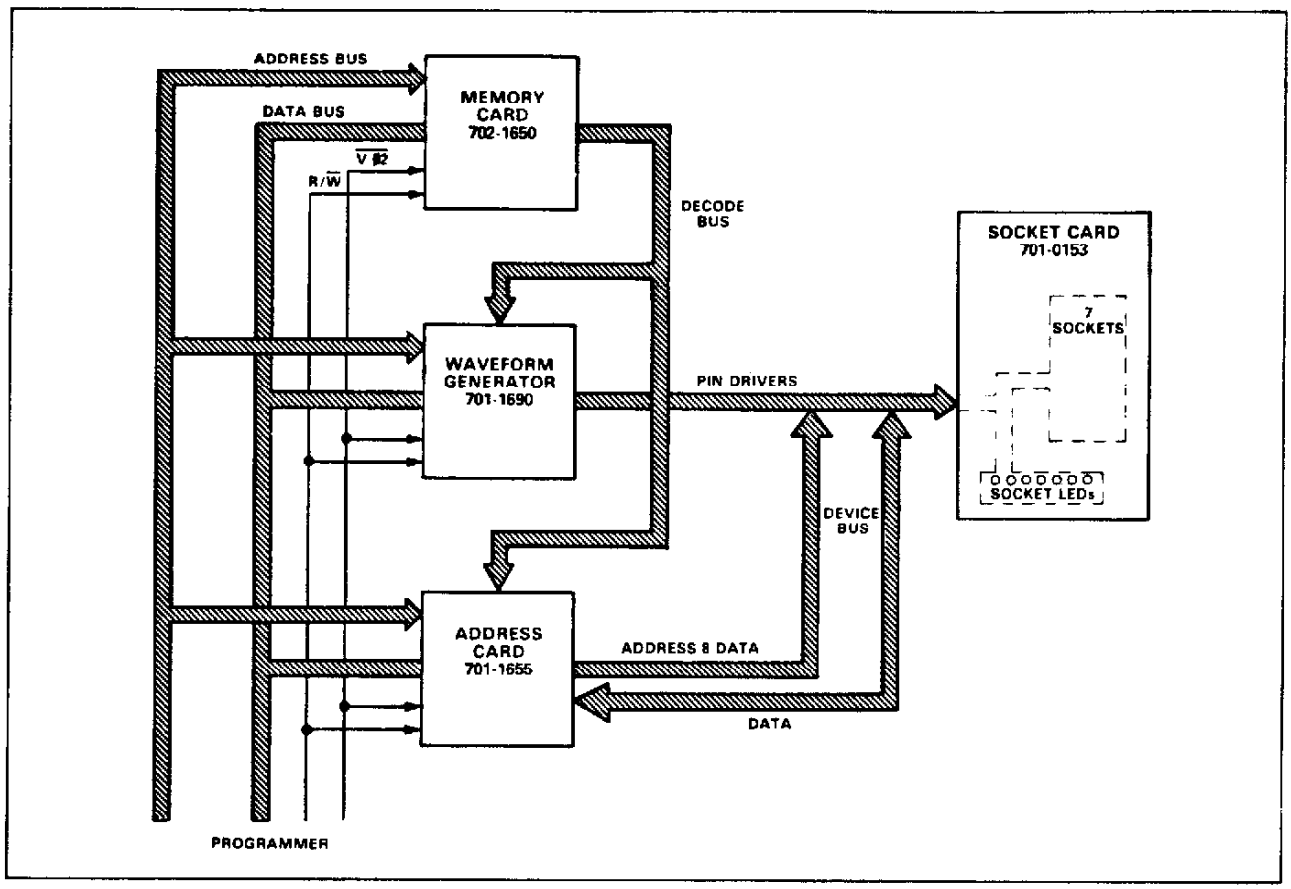


Figure 3-1. Block Diagram, UniPak 2B Electronics

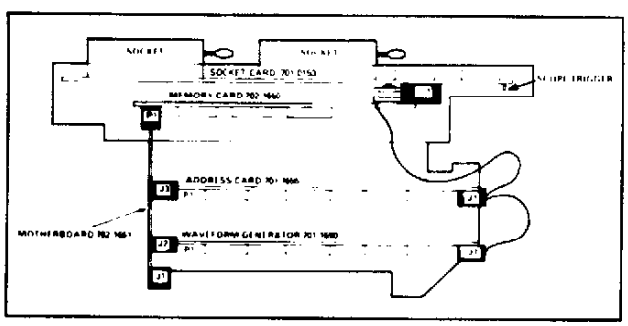


Figure 3-2. Principal Components

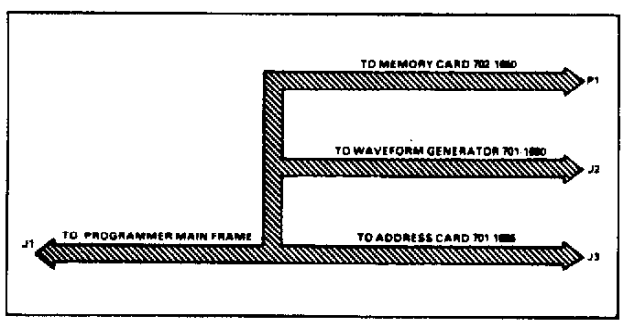


Figure 3-3. Motherboard Block Diagram

3.3.2 WAVEFORM GENERATOR

The waveform generator provides signals required for programming devices. These signals are generated by the blocks shown in figure 3-4.

Three major supplies are the V_{CC} supply, the $\overline{CE}$ supply and the bit supply, which are used to generate the respective signals. Each supply is software-controlled via a D/A converter. All DACs obtain their reference voltage from the DAC reference.

The V_{CC} waveforms are generated by writing appropriate DAC values from the firmware. The rise and fall times are fixed by the slewing rate of the op amp. Two overcurrent detectors are included, one for low currents and one for high currents (above 1.2 amps). If a detector is activated, the control latch is reset; the DAC-reference kill output then causes the DAC reference to go to zero, in turn causing all supplies to return to zero.

The V_{CC} supply senses the V_{CC} voltage at the PROM socket via the V_{CC} sense line. This remote sensing compensates for all cable drops between the supply and the socket.

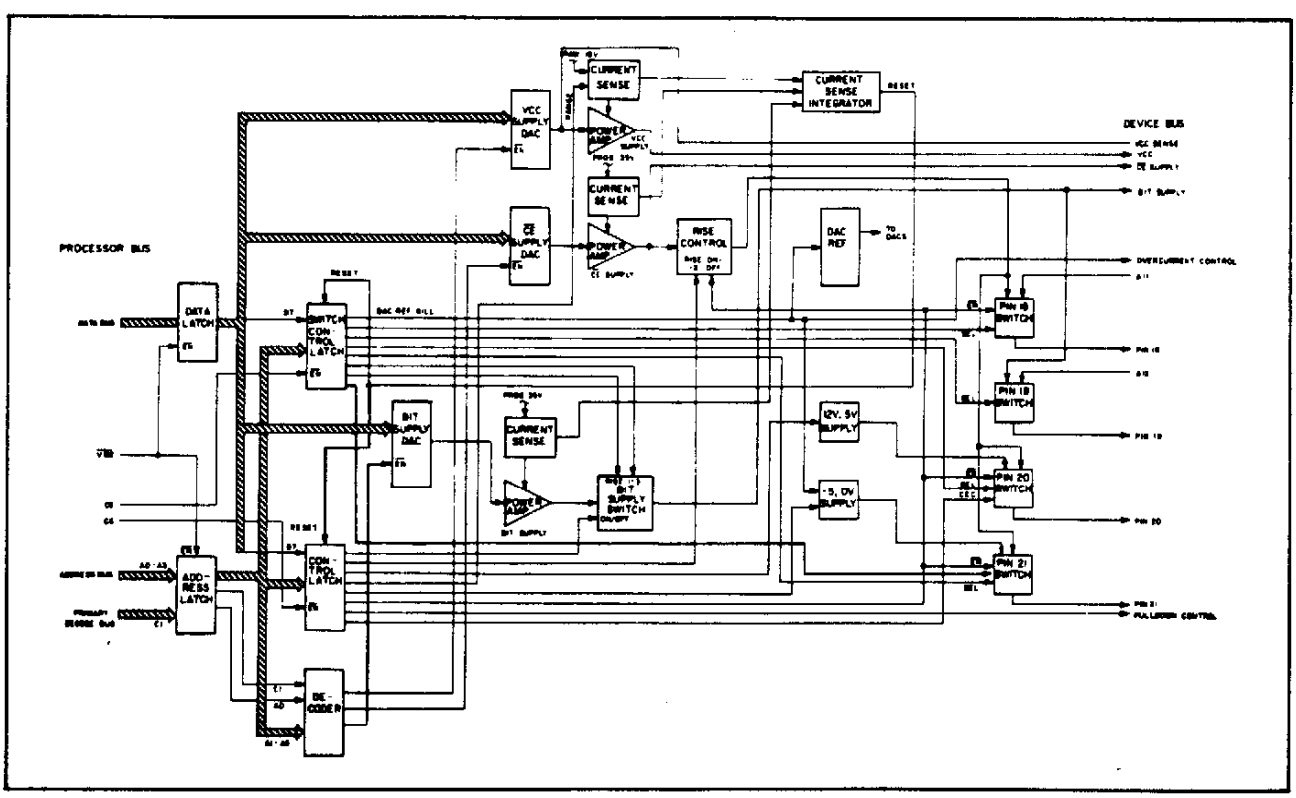


Figure 3-4. Waveform Generator Block Diagram

The $\overline{CE}$ waveforms are generated by using the $\overline{CE}$ supply in conjunction with one of the pin switches. The voltage level is selected by writing the appropriate value to the $\overline{CE}$ DAC. One of two rise times is selected by the control latch and rise-time control circuitry. Either the pin 18, 20 or 21 switch can be enabled by the switch-control latch to output the high-level $\overline{CS}$ voltage. Switches that are not enabled can output TTL levels.

Each pin switch consists of an emitter follower with the collector tied to the $\overline{CE}$ supply. A current source is provided for the base of each switch to charge the common rise-time capacitor. When the base is released, a linear ramp is generated which is truncated at the $\overline{CE}$ supply level. An NPN transistor pulldown is included in the switch to provide a 20 V/usec controlled fall time. Logic circuitry prevents the pulldown and pullup circuits from being active simultaneously.

The pin 21 switch uses the same principles as the pin 18 and pin 20 switches. However, a power amplifier output (0/-5V supply) provides the ground reference for the switch. For certain programming algorithms this amplifier output is brought to -5V.

The pin 20 switch includes a pullup that is connected to the +12V/+5V supply, thus allowing the switch in the TTL mode to switch from 0 to +12V as well as from 0 to +5V. The +12V/+5V supply consists of a monolithic regulator and a 5.1V zener diode controlled by the switch-control latch.

Signals to be applied to the data lines of a device are generated with the bit-supply signals and controlled by the bit-supply switch. The bit supply is nearly identical to the $\overline{CE}$ supply, but has one less diode in the feedback path, compensating for one less drop in the switch paths. The bit-supply switch consists of an emitter follower, a current source, and three rise-time control capacitors. The collector of the emitter follower is connected to the bit supply; the base is connected to the current source and timing capacitor. The control latch can select the timing capacitor and also control the base of the switch. When the base is released, the output ramps linearly to the bit-supply level. The output on the bit-supply switch is sent to the address card and to the pin 19 switch; unlike the pin 20, 21 and 18 switches, the pin 19 switch consists of a simple PNP-saturating switch controlled by the switch-control latch.

The current-sense integrator smoothes the transient overcurrent pulses occurring from charging supply capacitors. When an overcurrent condition from the V_{CC}, $\overline{CE}$, bit or (0/-5V) supply exists for sufficient time, the control latch is reset, in turn causing the DAC reference and the supplies to go to zero. The state of the overcurrent-control line can be read by the address card and used by the programmer to detect shorted devices. Table 3-1 lists the functions of the device-bus pins. The data latch buffers the data bus and holds data to satisfy the long DAC data-hold requirement. The address latch buffers the lower-order address lines and the primary decode bus. These buffered lines are then sent to the decoder and the address latches. The decoder provides decode signals to the DACs for the V_{CC}, $\overline{CE}$ and bit supplies. The switch-control latch and the control latch receive their clocks from a decoder on the address card.

Table 3-1 Pin Functions, Device Bus (at J1)

Pin	Function	Pin	Function
1	PA_8	26	PA_7
2	PA_9	27	PA_6
3	PA_{10}	28	PA_5
4	PA_{11}	29	PA_4
5	PA_{12}	30	PA_3
6	PA_{13}	31	PA_2
7	PA_{14}	32	PA_1
8	PA_{15}	33	PA_0
9	GND	34	V_{CC}
10	V_{CC} Sense	35	GND
11	$\overline{CE}$ Supply	36	GND
12	Bit Switch	37	Bit Supply
13	Pin 20	38	Pin 18
14	Pin 21	39	Pin 19
15	Scope Trigger	40	PD_1
16	-9V	41	PD_2
17	+24V	42	PD_3
18	$\overline{\text{Overcurrent}}$	43	PD_4
19	Pull-Down Control	44	S1
20	$\overline{V_{CC}}$ Pull-Up Control	45	S2
21	Address Supply +5V Select	46	S3
22	PD_8	47	$\overline{V_{CC}}$ Pulse
23	PD_7	48	Address DAC
24	PD_6	49	+5V
25	PD_5	50	Bit Switch Control

3.3.3 ADDRESS CARD

The address card, illustrated in figure 3-5, provides the device address, device data, data loads and supply measurement capability of the UniPak 2B.

The address drivers consist of addressable latches driving the device address bus. The addressable latches receive data from the most-significant-bit line of the data bus.

The data switch register drives PNP data switches which direct the output of the bit switch to the appropriate device-data line. The PNP switches are driven by current sources to provide a constant-base drive at all bit-switch voltages.

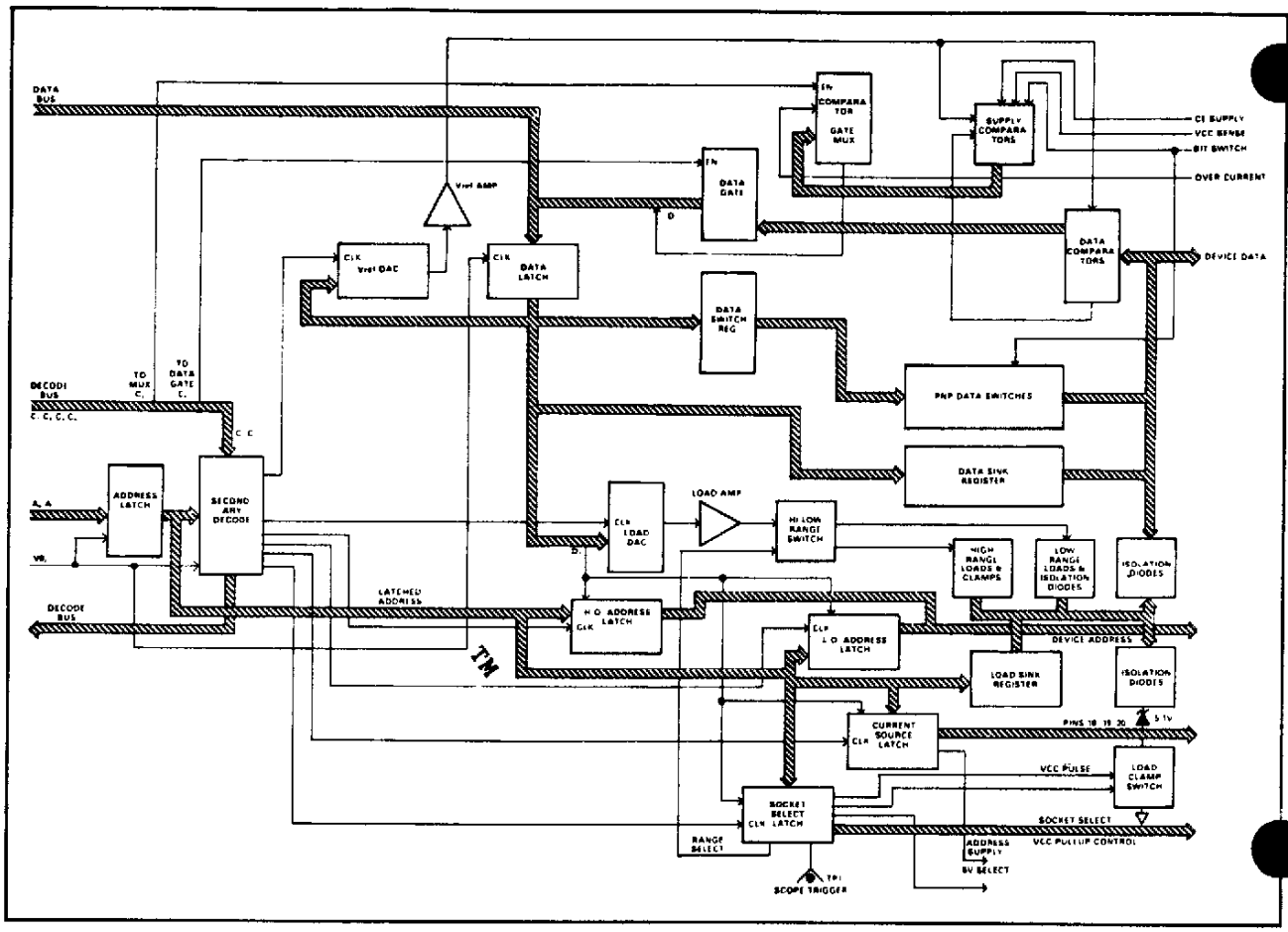


Figure 3-5. Address Card Block Diagram

The data sink register is used to shunt programming currents to ground. Device data is read via the data comparators and strobed to the processor bus via the data gate. The comparators receive their reference voltage from the V_{REF} amplifier, which is controlled by the V_{REF} DAC. Loading the device data bus is controlled by the load DAC, the load amplifier and the high/low-range load switch. This supply develops a voltage that is applied to either the low-range or high- and low-range load resistor banks. These resistors are fed through isolation diodes, which are connected to the device data pins. The load sink register enables the UniPak 2B to select which device data pins will have loads applied to them. The diode clamps limit the voltage applied by the load resistors to the data bus to approximately 5V when the load clamp switch is closed.

The supply comparators read the V_{CC} -sense line, the $\overline{CE}$ supply and the bit-switch line. The comparator gate/multiplexer strobes the data from the supply comparators and the overcurrent-read line to the most significant-bit line of the data bus.

The socket-select latch provides a control line for the high-/low-range switch and control lines for the socket card.

The data latch buffers the data bus and holds data to satisfy the DAC requirements.

The current source latch will supply a 4-mA current to a device provided there is a 15V zener diode inside the device on pin 18, 19 or 20. The address supply 5V select determines whether the address supply DAC or a fixed 5V will be applied to PA0-PA3.

The address latch buffers low-order addresses for the secondary decoder. The secondary decoder provides the appropriate signals for the DACs and registers, as well as the latches on this card and on the waveform generator. The $\overline{V \cdot 0}_2$ signal controls the timing of the various clock signals developed by the decoder.

The address card contains a jumper that signals the programmer whether the installed UniPak is a UniPak 2^{TM} or UniPak 2B model.

3.3.4 MEMORY CARD

The UniPak 2B memory card is shown in figure 3-6. EPROMs which store the UniPak 2B firmware are contained on the memory card. These EPROMs connect to the address bus directly and to the data bus through data buffers.

Paging is used when the 16K x 8 PROMs are installed. Two EPROMs and a latch comprise the primary decoding for the entire UniPak 2B. The EPROMs connect to the 12 high-order address lines and the R/$\overline{W}$ line. Outputs from the primary-decoder latch connect to the secondary decoder and also to secondary decoders on the address card and the waveform generator. A 1-of-8 decoder, timed with $\overline{V \cdot 0}_2$, provides the secondary decoding for the software EPROMs. Two additional lines from this decoder connect to the address card to provide the decode signals for the data gate and comparator gate/multiplexer. Additional outputs from the binary decoder enable the data buffer during all software-read operations and lower the data gate enable line during any access of the UniPak 2B.

The pulse generator consists of a count-up ripple counter, an 8-bit latch, and a 10-mHz crystal-controlled clock. The latch is connected to the data bus and is used to load the counter, allowing the pulse generator to be programmable between 0.1 and 25.5 us.

The current source consists of a fixed 20-mA current source and a programmable current source. The control logic selects which current source is active. The pulse generator can be selected to control the programmable current source.

The address supply generates the voltage necessary to drive the CMOS buffers located on the socket card. The voltage is generated from the 24V power supply using an NPN transistor driven by an op amp. The input of the op amp is a DAC, which allows the voltage to be software selectable.

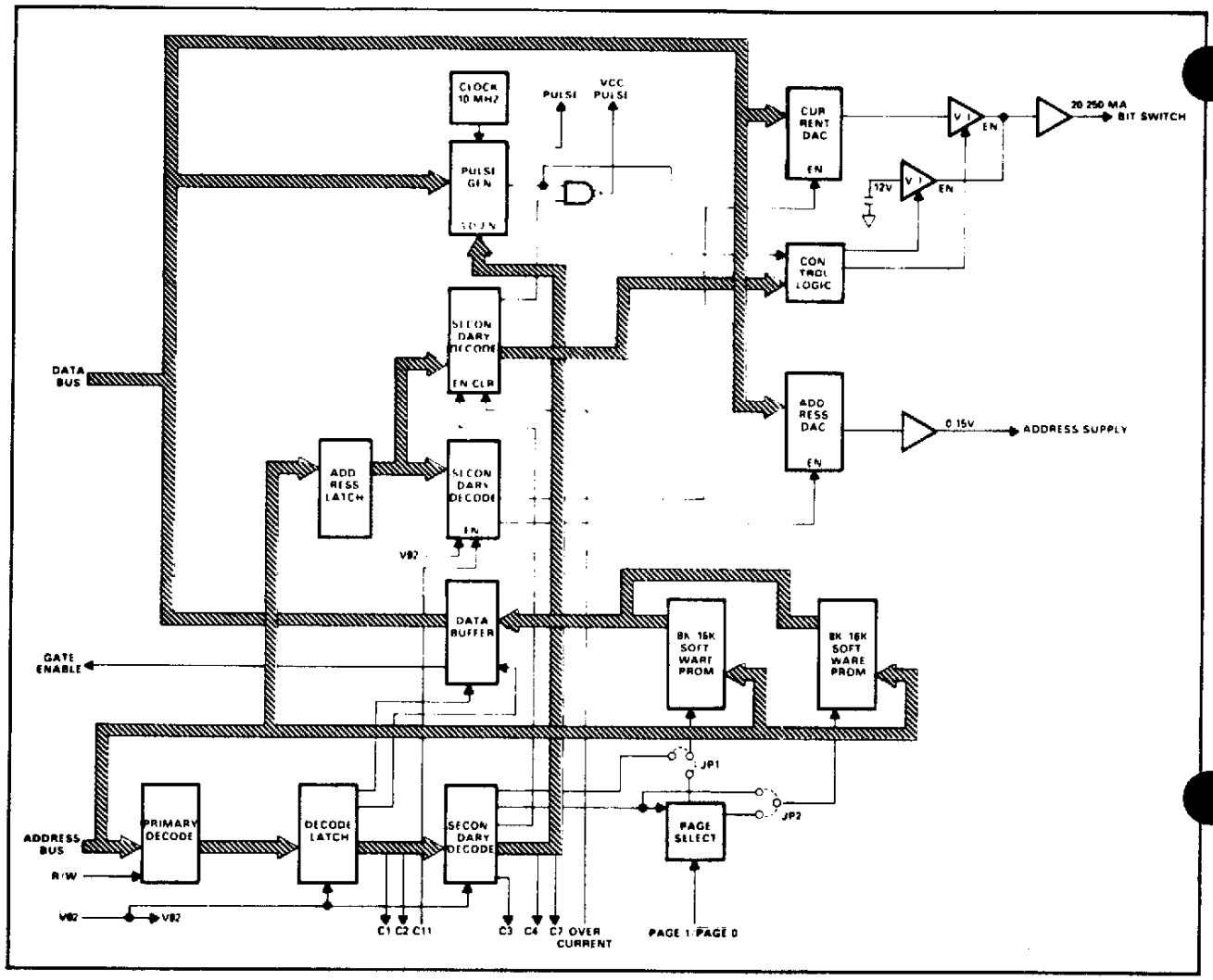


Figure 3-6. Memory Card Block Diagram

3.3.5 UNIPAK 2B SOCKET CARD

The socket card distributes to the device sockets the signals developed on the address card and the waveform generator (refer to figure 3-7).

The device address bus (PA0-PA15) is generated on the address card and fed to the socket card via the ribbon cable. On the socket card, the bus is fed into CMOS buffers. The address supply DAC connects to the V_{DD} supply on these buffers. This allows the VOH level to be under DAC control. The address supply 5V select line allows PA0-PA3 to switch at TTL levels while all other address lines switch between "0" and the address supply level. The address clamps provide overvoltage protection and are connected to a comparator that senses overvoltage, shutting down all the supplies when excessive voltage is detected.

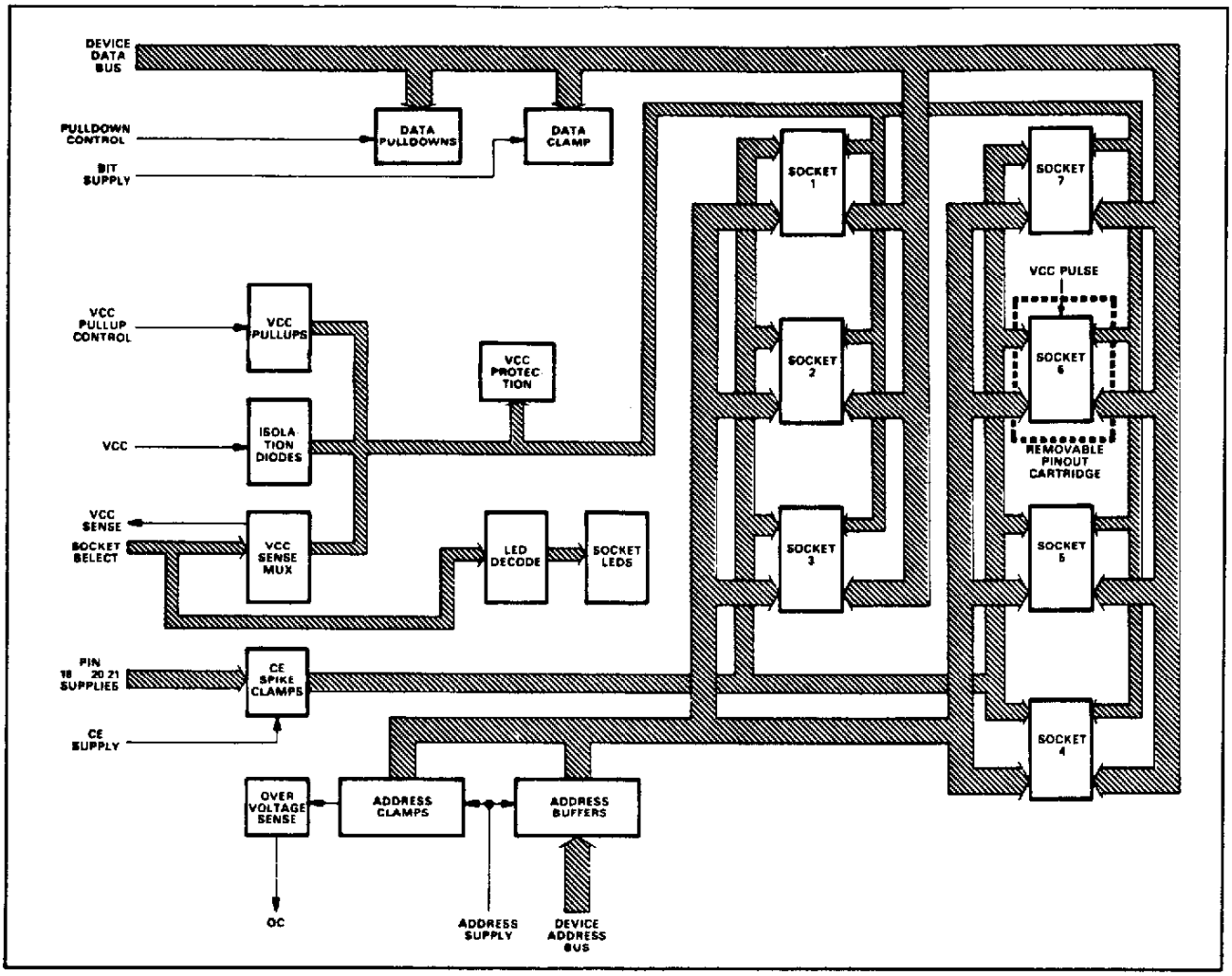


Figure 3-7. Socket Card Block Diagram

The device-data bus connects directly to all sockets. Four-bit devices are connected to PD1-PD4. The data pulldowns consist of 1 kohm resistors and a diode network. The data clamp has two modes of operation controlled by the bit switch control line.

When voltage pulses are being applied to a device, the pass element of the data clamp is switched out of the circuit. The op amp and 2.2 kohm resistor precharge the 0.1 uF capacitors to the level set by the bit supply so that the network does not absorb energy from the actual data-line programming pulses.

When current pulses are being applied to a device, the pass element is switched into the circuit. The data clamp will be set to a voltage level by the bit supply and will sink all unnecessary current.

Pins 18, 19, 20 and 21 of the 24-pin device socket receive signals directly from the waveform generator via the corresponding pin switches. A spike-suppression network is provided for pins 18, 20 and 21 where the $\overline{CE}$ supply charges the RC network. V_{CC} is applied to all sockets through seven diodes. Remote sensing of the voltage at the selected socket is provided by the analog switch of the V_{CC} -sense multiplexer. When V_{CC} is brought to zero, the device's V_{CC} lines can be pulled up by the V_{CC} pullups. The V_{CC} sense-multiplexer and a comparator on the address card are then used to read the V_{CC} voltage. If a device is properly inserted in a socket, the V_{CC} voltage will be above 2V. If it is in backwards it will be below 1V, and if no device is in the socket, the voltage will approach 4V.

The LED decoder is used to light the LEDs below the selected socket.

3.3.6 PINOUT CARTRIDGES

The pinout cartridges follow the same basic design, varying only to conform to the individual socket design, with the exception of the 40-pin 1024k bit pinout cartridge, which has some additional circuitry. All of the pinout cartridges have a card edge connector to mate with the socket board, a shift register that outputs to the UniPak 2B the number of the pinout cartridge, a diode to illuminate when the socket is selected, data line diode clamps, the applicable socket, and land patterns to route the data from the card edge connector to the appropriate socket pin. Additional circuitry on pinout cartridge no. 11 (40-pin socket) includes buffers and latches to split the address and data lines into a high and low order. Refer to the schematic in Appendix B of the installed pinout cartridge for individual details.

SECTION 4

MAINTENANCE

4.1 INTRODUCTION

This section covers maintenance for the UniPak 2B. Included are assembly, disassembly, cleaning, and preventive maintenance. Each is covered in one of the following subsections.

4.2 UNIPAK 2B DISASSEMBLY

To disassemble the UniPak 2B, refer to figure 4-1 and follow the proccdure below.

1. Remove the UniPak 2B from the programmer; see section 2 for details.

2. Place the UniPak 2B face down on a flat surface.

3. Unscrew the captive fasteners (figure 4-1a) until they hang loosely; the screws will not separate from their standoffs.

4. Lift the card cage up slightly, then pull out (as shown in figure 4-1b) to unlock the flanges.

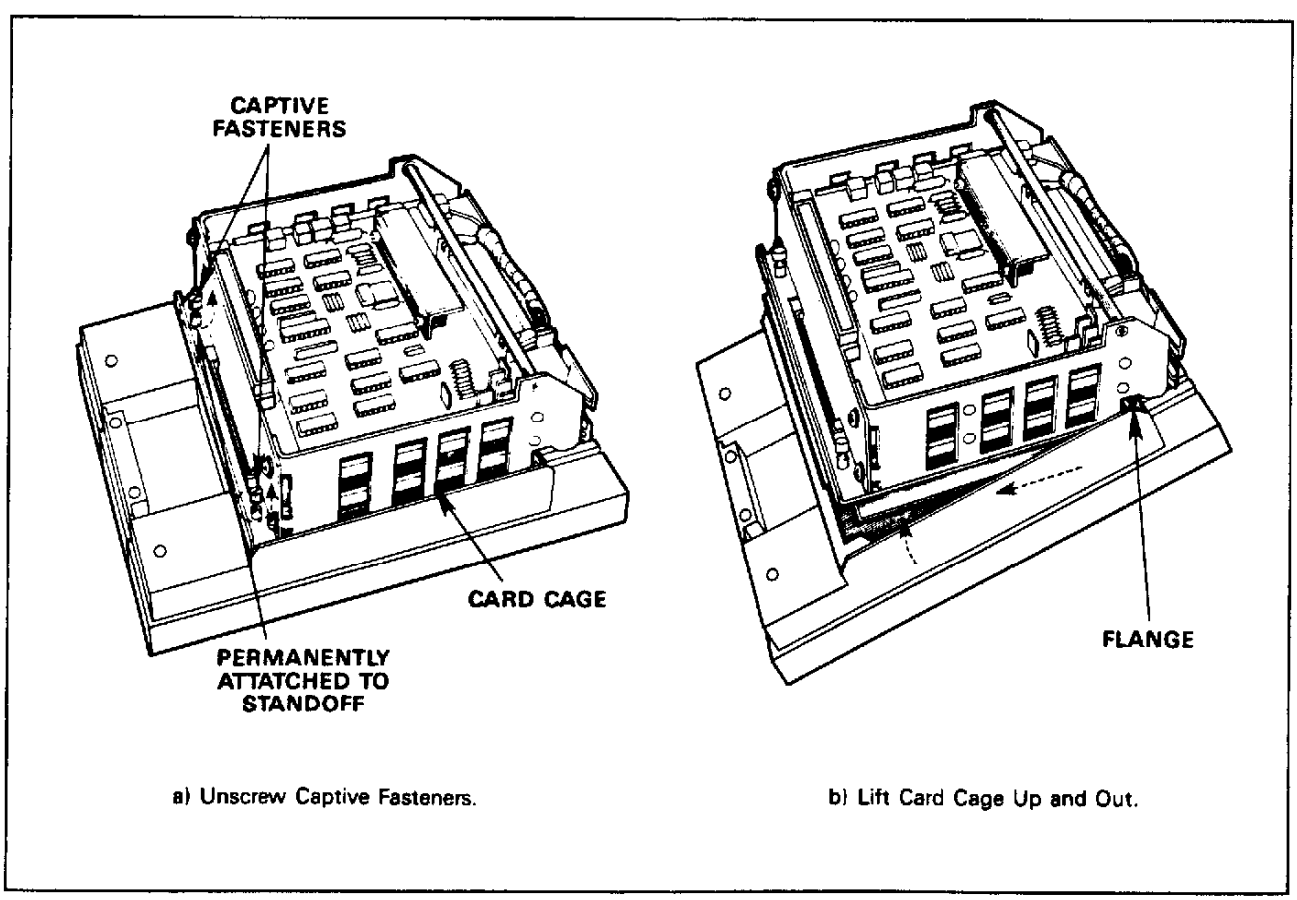


Figure 4-1. UniPak 2B Disassembly

5. Lift the card cage up until you can see the socketboard interconnect cable and its connector (figure 4-2).

6. Flip the extraction tabs out on each side of the connector (figure 4-2).

7. Pull the cable out of the connector.

8. Disconnect the ground wire from the socketboard (see figure 4-2).

9. Flip the extraction tabs out on the top card (waveform generator card) and unplug the interconnect cable from its connector (figure 4-3).

10. Flip the extraction tabs out on the top card (waveform generator card).

11. Pull the waveform generator card out along the guides (figure 4-3).

12. Repeat steps 9, 10, and 11 for the extraction tabs on the address card.

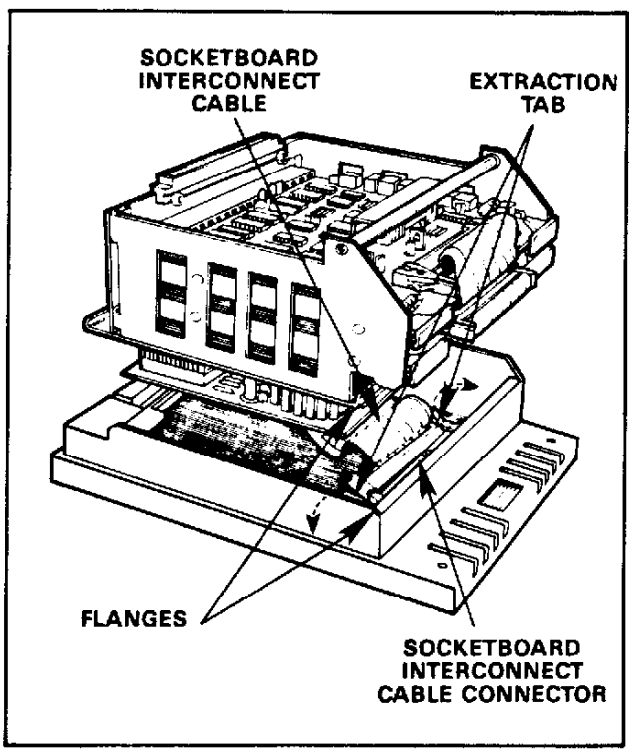


Figure 4-2. Socket Board Interconnect Cable Disconnect

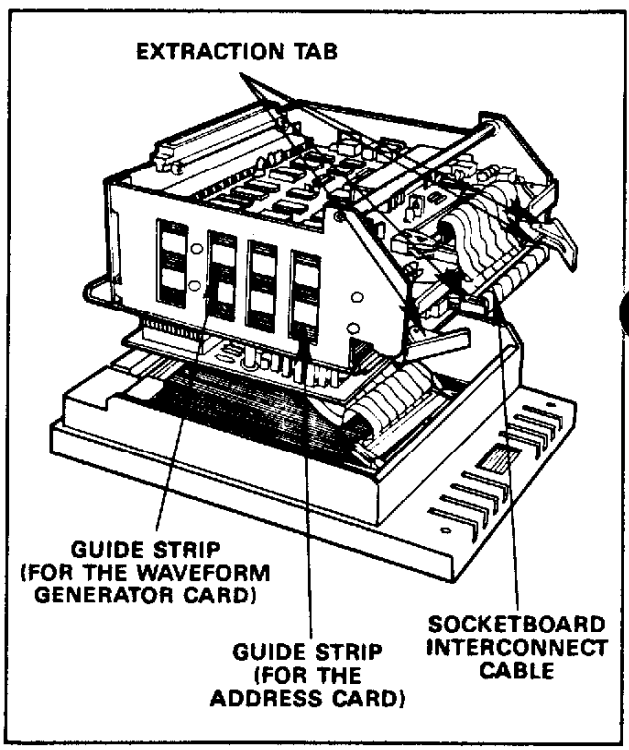


Figure 4-3. Circuit Board Removal

13. Remove the two screws and the shield, and pull the memory card down to unplug it from the edge connector (as shown in figure 4-4).

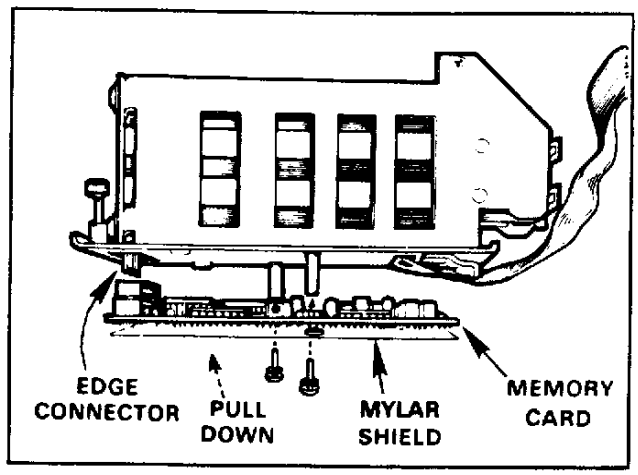


Figure 4-4. Memory Card Removal

4.3 UNIPAK 2B ASSEMBLY

1. Plug the memory card onto its edge connector, as shown in figure 4-4.

2. Replace the shield and the two screws.

3. Flip the two extraction tabs down on the address card.

4. Using the flat surfaces of the extraction tabs, gently push the address card along the guides into its connector.

5. Make sure the extraction tabs on the interconnect cable connector are flipped open.

6. Firmly, but gently, push the socketboard interconnect cable into the connector. Notice that the extraction tabs will move back to their locked positions when the cable is locked into the connector.

7. Repeat steps 3 through 6 to replace the waveform generator card.

8. Reconnect the ground wire to the socketboard.

9. Plug the socketboard interconnect cable into its connector on the socketboard (figure 4-2).

10. Replace the card cage by tilting it up to lock the flanges, as shown in figure 4-1, then gently setting it down. Make sure the captive fasteners line up with the fastener holes on the UniPak 2B frame.

11. Tighten the captive fasteners finger tight.

4.4 CLEANING

Inspect the UniPak 2B inside and out for accumulated dirt or dust. To clean the UniPak 2B, follow the procedure below.

1. Wipe any dust and/or dirt off the outside of the UniPak 2B with a clean, damp cloth.

NOTE

Do not use abrasive cleaners or solvents. They will damage the case.

2. Remove dust from the circuit boards with a blast of dry, compressed air or a clean, soft-bristled brush.

4.5 PREVENTIVE MAINTENANCE

Periodically visually inspect your UniPak 2B. Check the cable connections, card seating, the mounting of socketed components, for open or damaged land patterns, for heat-damaged components, etc. Also check for shorts, opens or unstable continuity. If you find heat-damaged components, identify and correct the cause of the overheating to prevent further damage.

SECTION 5

CALIBRATION

5.1 INTRODUCTION

The need for calibration varies with the amount of use your UniPak 2B receives. Generally, we suggest calibration whenever any of the following apply:

1. Programming yields fall below the manufacturer's recommended minimums.

2. Troubleshooting has resulted in the replacement or adjustment of some component in the system.

3. The user's company policy requires periodic calibration certification.

NOTE

If calibration or repair is required but you lack the facilities to accomplish it, contact the nearest Data I/O Service Center.

Because of differences in programmer mainframes, this manual does not attempt to cover all areas of programmer calibration. Instead, it lists the steps necessary to calibrate only the UniPak 2B.

Calibration of the UniPak 2B consists of three parts:

1. Power Supply Calibration measures the DC supply voltages of the programmer. All other voltages depend on these supplies; therefore, this part of the calibration procedure must be done first. Refer to your programmer manual.

2. DC Calibration consists of measuring and adjusting critical DC voltage levels generated by the UniPak 2B.

3. Waveform Observation (optional) enables observation of waveforms on an oscilloscope to ensure compliance with the device manufacturers' critical voltage and timing specifications.

NOTE

The optional waveform test are required only if the instrument consistenly gives low yields even after calibration. They will provide tests at individual family/pinout codes. The material for these tests are not included with this reference data. They are avalable upon request from the Data I/O corporate service department. Please include a list of the family/pinout codes for which you desire waveforms with your request.

The first part of the calibration procedure (power supply calibration) varies with the type of programmer you have. Therefore, this manual refers you to your programmer manual for details on power supply calibration. DC calibration is discussed in section 5.2. The optional verify voltage checks and the optional waveform observation are available upon request.

The following equipment is necessary to calibrate the UniPak 2B:

- Data I/O calibration extender (part number 910-1521)
- Three and a half-digit digital voltmeter (DVM). The dcV accuracy of the DVM must be ±0.25% or better.
- Dual-trace oscilloscope (Tektronix 465 or equivalent)

Check the appropriate programmer manual for any additional equipment that you may need to calibrate the programmer.

To prepare your UniPak 2B for calibration, follow the procedures outlined below.

1. Turn the programmer power off (see the programmer manual for details).
2. Remove the UniPak 2B from the programmer; see section 2 for details.
3. Insert the calibration extender into the programmer the same way you insert the UniPak 2B (see section 2).
4. Unscrew the two thumb screws (captive fasteners) located on the underside of the top cover of the UniPak 2B (figure 4-1); they connect the card cage to the socket assembly. Separate the two parts of the assembly.

CAUTION

Do not let the fasteners short to the motherboard.

5. Insert the 64-pin connector of the card cage into the mating connector on the calibration extender (figure 5-1b).
6. Lean the top portion of the UniPak 2B against its bottom portion at a 45-degree angle (see figure 5-1).

NOTE

Be sure the socket assembly flange locks the card cage flange (see figure 5-1a). Do not allow the frame of the socket assembly to short to the memory board. Be careful not to strain the cable or scratch the top of the programmer.

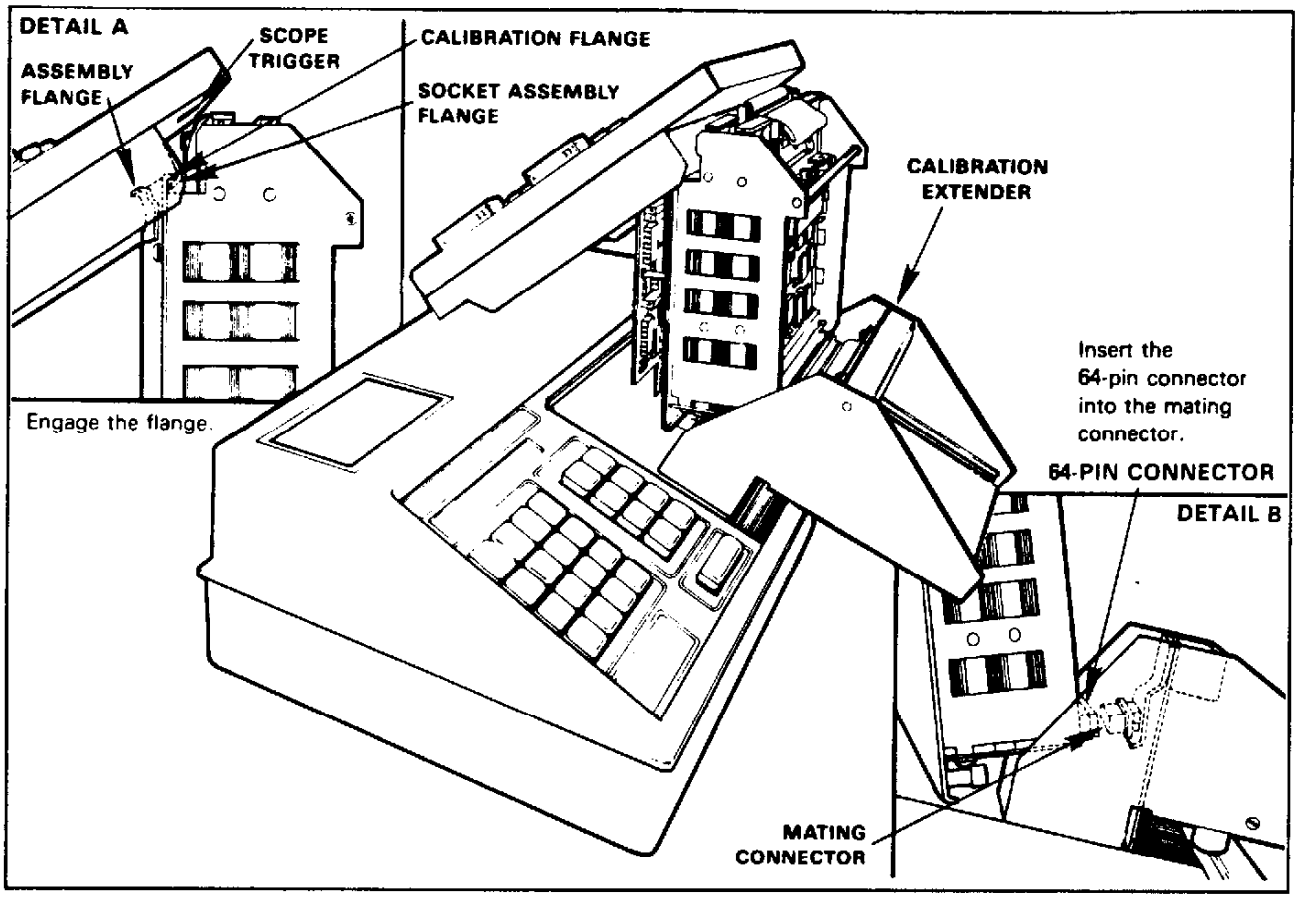


Figure 5-1. Calibration Setup

5.2 DC CALIBRATION

The DC calibration procedure described in this section enables you to adjust critical DC voltage levels generated by the UniPak 2B. To follow this procedure, use the measurement chart (table 5-1) located at the end of this section. The measurement chart contains the information needed for all DC calibration tests. The information is included on the measurement chart in columns with the following headings:

- Step No. tells which step to use for each test. Step numbers are set at the programmer keyboard and reflected in the display.
- Test No. identifies individual tests.
- Test Description identifies the functions being tested.
- Measurement Test Location tells which socket pins, circuit boards, or test points to probe for measuring voltages.

- Measurement specifies allowable measurement ranges. If a reading falls outside the range and you cannot adjust it to within the range, do not use the UniPak 2B until the problem is corrected.

- Adjustment Location tells which potentiometer to adjust if a measurement is out of range.

- Comments gives special instructions for particular tests.

The DC calibration procedure is as follows:

CAUTION

Remove all devices from the sockets before entering the calibration mode (see section 2 for details). Waveform generation may damage any device in the UniPak 2B sockets.

1. Turn the programmer power on (see the programmer manual).

2. Put the programmer into the calibration mode by following the key sequences in table 5-2.

Table 5-2 Key Sequence to Access the Calibration Mode

Programmer System	Key Sequence To: Enter Calibration Mode	Increment Step No.	Decrement Step No.
19	Press SELECT Press C2 Press ENTER Enter Step Number* Press Start	Press ENTER	Press REVIEW
29A/29B	Press SELECT Press C1 Press START Enter Step Number* Press Start	Press START	Press REVIEW
100A	Press SELECT Press 12 Enter Step Number* Press Start	Press START	Press BACKSPACE

*Optional

3. Perform the calibration steps on the measurement chart (table 5-1). For steps 5, 6, and 7, refer to figures 5-4 through 5-10 located at the end of the measurement chart to observe the bit switch rise waveform, the DAC step waveforms, and the current DAC step waveform.

For each general calibration step on the measurement chart do the following:

- Take measurement readings at the device sockets or test points indicated on the measurement chart; figure 5-2 shows the pin numbers for the sockets; figure 5-3 shows test points.
- Ground the digital voltmeter to socket 7, pin 8 on the front panel of UniPak 2B.
- The adjustment pots on the waveform generator, memory board, and the address card enable you to make adjustments when your measurements do not match the measurement chart; figure 5-3 shows the location of these adjustment points.

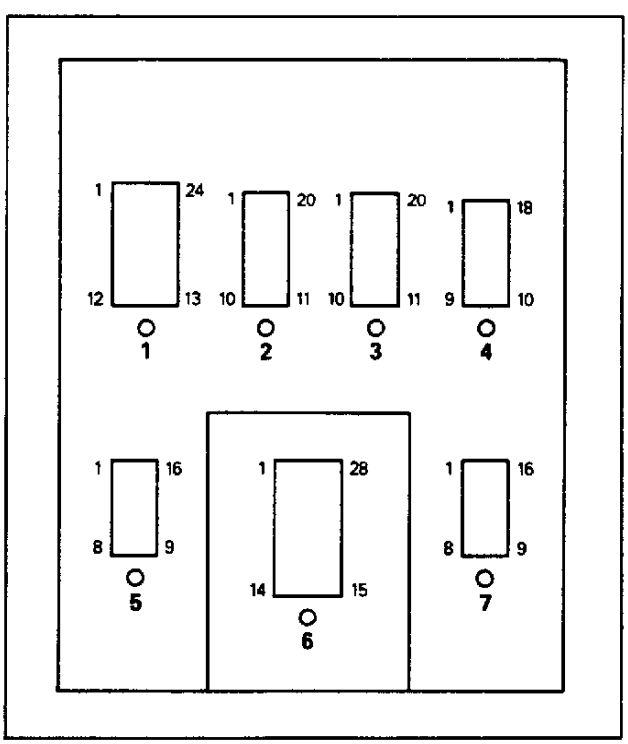


Figure 5-2. Pin Numbers of Device Sockets

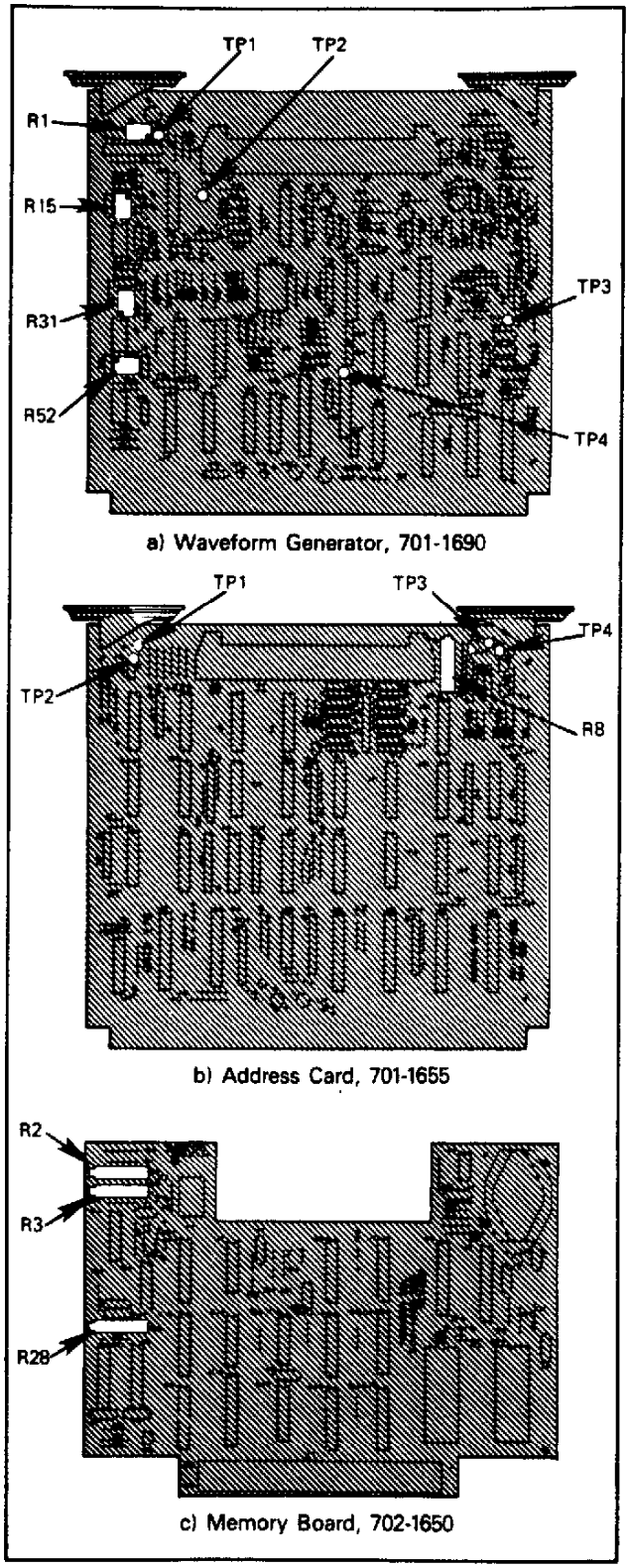


Figure 5-3. Adjustment Locations

- Access each new step by pressing the START (or ENTER) key. The new step number will appear in the display when the UniPak 2B is ready for the next step. To go back to a previous test, press the REVIEW (or BACKSPACE) key.

Table 5-1 Measurement Chart

STEP	TEST NO.	TEST DESCRIPTION	MEASUREMENT LOCATION	MIN	MEASUREMENT NOM	MAX	ADJUSTMENT LOCATION	COMMENTS
01	01	V reference supply	Card 701-1655 TP2	14.40 V	14.5 V	14.60 V	R8, 701-1655	
	02	Load supply (high range)	Card 701-1655 TP4	25.0 V		26.0 V		
	03	Load Supply (low range)	Card 701-1655 TP3	25.0 V		26.0 V		
	04	Vcc Supply	Socket 1 Pin(s) 24	11.90 V	12.0 V	12.10 V	R52, 701-1690	
	05	CE Supply	Socket 1 Pin(s) 20	32.7 V	33.0 V	33.2 V	R15, 701-1690	
	06	Bit Supply	Socket 1 Pin(s) 9	25.7 V	26.0 V	26.2 V	R31, 701-1690	
	07	Address Supply	Socket 1 Pin(s) 8	14.8 V	15.0 V	15.2 V	R28, 702-1650	
02	08	V reference supply	Card 701-1655 TP2	6.70 V		6.90 V		
	09	Load Supply	Card 701-1655 TP3	10.3 V		11.7 V		
03	10	V reference supply	Card 701-1655 TP2	3.30 V		3.50 V		
	11	Current source 20 mA	Socket 1 Pin(s) 9	19.5 mA	20.0 mA	20.5 mA	R3, 702 1650	Use a 100-ohm, 2W carbon comp resistor in series with the current meter
04	12	Current source supply	Socket 1 Pin(s) 9	118.0 mA	120.0 mA	122.0 mA	R2, 702-1650	Use a 100-ohm, 2W carbon comp resistor in series with the current meter
05	13	Bit switch rise waveform	Socket 1 Pin(s) 14				R1, 701 1690	See waveform in figure 5-4
06		DAC Step Waveforms						
	14	Vcc	Socket 1 Pin(s) 24					See waveform in figure 5-5
	15	Bit Supply	Card 701-1690 TP2					See waveform in figure 5-6
	16	CE Supply	Card 701-1690 TP1					See waveform in figure 5-7
	17	Vref Supply	Card 701-1655 TP2					See waveform in figure 5-8
	18	Load Supply	Card 701-1655 TP3					See waveform in figure 5-9
07	19	Current DAC step waveform	Socket 1 Pin(s) 9					Place a 200-ohm, 5W resistor between pins 9 and 12 of socket 1 (See figure 5-10)
08	20	All voltages off	All sockets All pins	-0.1 V		0.4 V		
09	21	Socket 1 LED						Confirm the socket 1 LED is on
	22	Vcc Supply load	Socket 1 Pin(s) 24	11.8 V		12.1 V		Place a 20-ohm, 2W resistor between pins 24 and 12 of socket 1
10	23	No Operation						
11	24	CE Supply load	Socket 1 Pin(s) 20	32.3 V		33.2 V		Place a 100-ohm, 10W resistor between pins 20 and 12 of socket 1
	25	Pin 18 voltage switch	Socket 1 Pin(s) 18	32.7 V		33.2 V		
	26	Pin 21 voltage switch	Socket 1 Pin(s) 21	32.7 V		33.2 V		
12	27	Bit supply Load	Socket 1 Pin(s) 11	25.2 V		26.0 V		Place a 100-ohm, 5W resistor between pins 11 and 12 of socket 1
	28	Pin 19 voltage switch	Socket 1 Pin(s) 19	25.6 V		26.2 V		
13	29	Vcc voltage linearity	Socket 1 Pin(s) 24	3.90 V		4.10 V		
	30	CE Supply linearity	Socket 1 Pin(s) 18	23.0 V		23.5 V		Place a 2.2 Kohm, 1/2W resistor between pins 12 and 18 of socket 1
	31	Address Supply	Socket 1 Pin(s) 8	4.70 V		5.30 V		
	32	-5V Supply	Socket 1 Pin(s) 21	-5.2 V		-4.8 V		
	33	12V Supply	Socket 1 Pin(s) 20	11.4 V		12.6 V		
	34	Clamp Supply	Socket 1 Pin(s) 11	20.5 V		21.5 V		
	35	Current source linearity	Socket 1 Pin(s) 11	88.0 mA		92.0 mA		Use a 100-ohm, 2W carbon comp resistor in series with the current meter
14	36	Vcc voltage linearity	Socket 1 Pin(s) 24	4.90 V		5.10 V		
	37	CE Supply linearity	Socket 1 Pin(s) 21	11.4 V		12.0 V		
	38	Clamp Supply linearity	Socket 1 Pin(s) 9	6.7 V		7.3 V		

Table 5-1 Measurement Chart (continued)

STEP	TEST NO.	TEST DESCRIPTION	MEASUREMENT LOCATION	MIN	MEASUREMENT NOM	MAX	ADJUSTMENT LOCATION	COMMENTS
15	39	Vcc voltage linearity	Socket 1 Pin(s) 24	5.90 V		6.10 V		
	40	I source and pulldowns	Socket 1 Pin(s) 9,11,14,16	2.0 V		2.6 V		
	41	I source and pulldowns	Socket 1 Pin(s) 10,13,15,17	0.0 V		1.0 V		
16	42	I source and pulldowns	Socket 1 Pin(s) 10,13,15,17	2.0 V		2.6 V		
	43	I source and pulldowns	Socket 1 Pin(s) 9,11,14,16	0.0 V		1.0 V		
17	44	Pinout Cartridge #1 LED						Confirm that socket 6 LED is on
	45	Vcc voltage supply	Socket 6 Pin(s) 28	4.90 V		5.10 V		
	46	Odd address and data high	Socket 6 Pin(s) 2,3,5,7,9, 11,13,16,18,20,22,24,26	3.5 V		6.0 V		
	47	Even address and data low	Socket 6 Pin(s) 1,4,6,8,10, 12,15,17,19,21,23,25,27	-0.1 V		0.4 V		
18	48	Odd address and data low	Socket 6 Pin(s) 2,3,5,7,9, 11,13,16,18,20,22,24,26	-0.1 V		0.4 V		
	49	Even address and data high	Socket 6 Pin(s) 1,4,6,8,10, 12,15,17,19,21,23,25,27	3.5 V		6.0 V		
19	50	Odd data lines high	Socket 6 Pin(s) 11,13,16,18	25.5 V		26.5 V		
	51	Even data lines pullups	Socket 6 Pin(s) 12,15,17,19	4.5 V		5.5 V		
20	52	Odd data lines pullups	Socket 6 Pin(s) 11,13,16,18	4.5 V		5.5 V		
	53	Even data lines high	Socket 6 Pin(s) 12,15,17,19	25.5 V		26.5 V		
21	54	Socket 2 LED						Confirm that socket 2 LED is on
	55	Vcc voltage supply	Socket 2 Pin(s) 20	4.90 V		5.10 V		
22	56	Socket 7 LED						Confirm that socket 7 LED is on
	57	Vcc voltage supply	Socket 7 Pin(s) 16	4.90 V		5.10 V		
23	58	Socket 5 LED						Confirm that socket 5 LED is on
	59	Vcc voltage supply	Socket 5 Pin(s) 16	4.90 V		5.10 V		
24	60	Socket 4 LED						Confirm that socket 4 LED is on
	61	Vcc voltage supply	Socket 4 Pin(s) 18	4.90 V		5.10 V		
25	62	Socket 3 LED						Confirm that socket 3 LED is on
	63	Vcc voltage supply	Socket 3 Pin(s) 20	4.90 V		5.10 V		
26	64	Vcc pullup 1 on	Socket 1 Pin(s) 24	4.0 V		5.2 V		
		Vcc pullup 2 on	Socket 2 Pin(s) 20	4.0 V		5.2 V		
		Vcc pullup 3 on	Socket 3 Pin(s) 20	4.0 V		5.2 V		
		Vcc pullup 4 on	Socket 4 Pin(s) 18	4.0 V		5.2 V		
		Vcc pullup 5 on	Socket 5 Pin(s) 16	4.0 V		5.2 V		
		Vcc pullup 6 on	Socket 6 Pin(s) 28	4.0 V		5.2 V		
		Vcc pullup 7 on	Socket 7 Pin(s) 16	4.0 V		5.2 V		

SECTION 6

TROUBLESHOOTING

6.1 INTRODUCTION

This section will help you interpret and isolate failures in the UniPak 2B. Use it in conjunction with section 3 (Circuit Description) and the schematics provided in the back of this manual.

There are three major classes of failures that can occur in a system comprised of a programmer and a UniPak 2B. The first is no system operation, the second is poor yields, and the third is UniPak 2B failure.

After successfully troubleshooting the UniPak 2B, you must calibrate it according to the instructions in section 5. It is very important that the programmer be calibrated before the UniPak 2B is calibrated.

6.2 NO SYSTEM OPERATION

You should perform the following steps if the system will not initialize with the UniPak 2B installed. After completing each step, determine whether the problem still exists.

1. Check to be sure the UniPak 2B is properly installed in your programmer.

2. Check the UniPak 2B programmer mating connector (J1) for bent or broken pins. (Pin HH is intentionally shorter.)

3. Check the UniPak 2B cards to be sure they are correctly installed in their connectors (refer to section 4).

4. Check the ribbon cable to be sure it is properly inserted in the connectors (refer to section 4).

5. Check the programmer power supplies for proper voltage output levels (refer to the programmer manual).

6. Check the ground cable connection.

7. If steps 1 through 6 fail to isolate the problem, contact your local Data I/O Service Center.

6.3 POOR YIELDS

Perform the following procedure if the yield rate begins to decrease. After completing each step, determine whether the problem still exists.

1. Calibrate the programmer (refer to the programmer manual).

2. Calibrate the UniPak 2B (refer to section 5).

If the poor yields persist contact your local Data I/O Service Center for assistance. They will provide service or, if you wish to continue the tests yourself, they will provide you, through the factory, with waveform and voltage tests for individual family/pinout codes. Please provide a list of the family/pinout codes that you require if you desire this service.

6.4 UNIPAK 2B FAILURE

Perform the following procedure if a device will not program at all, or if error messages are displayed. After completing each step, determine whether the problem still exists.

1. Check that the family and pinout codes are correct for the device, and that the device is being inserted in the correct socket.

2. If possible, try a known-good device to determine whether there is a hardware problem.

3. Check to be sure the UniPak 2B is properly installed.

4. Check the UniPak 2B programmer mating (J1) connector for bent or broken pins. (Pin HH is intentionally shorter.)

5. Check the UniPak 2B cards to be sure they are correctly installed in their connectors (refer to section 4).

6. Check to be sure the ribbon cable is correctly oriented and properly inserted in the connectors.

7. Check the ground cable connection.

8. Perform a complete calibration, noting any measurements falling outside the indicated limits. Refer to the corresponding test number in table 6-1 for suspected boards and components, as well as the circuit description (section 3) and the schematics (Appendix B), to attempt to isolate the problem.

9. Perform waveform observations and note any discrepancies. Referring to the circuit description and the schematics may be helpful in isolating the problem.

10. If steps 1 through 9 fail to resolve the problem, contact your local Data I/O Service Center.

Table 6-1 Troubleshooting Chart

TEST NO.	SUSPECT BOARDS	SUSPECT COMPONENTS
1	701-1655	VR1, U17, U25, R8
2	701-1655	VR1, U16, U25, Q1, Q2, Q3, R8
3	701-1655	VR1, U16, U25, Q2, R8
4	701-1690	U15, U7, U12, Q21, R52, CR15, CR16, VR1, Q15, U19, U20
	701-0153	CR26, U2, CR22
5	701-1690	U14, U7, U3, Q3, R15, CR4, CR3, U10, U9, U11, Q24, Q25, Q19, CR14, Q16, U18, U17, VR1, Q15, U19, U20
	701-0153	C15, R19, CR54
6	701-1690	U13, U7, U6, Q9, R31, CR10, CR11, Q2, CR19, U19, VR1, U20, Q15, Q25, U11
	701-1655	U23, R1, Q15, Q17, RP8, RP3, RP4, RP2, Q4, U24, U11, CR6
	701-0153	Q3, Q6, Q5, U3, Q4
7	702-1650	U23, U22, VR2, Q2, R28
	701-1655	U4, U14, U20
	701-0153	CR19, Q1, U6
8	701-1655	VR1, U17, U25, R8
9	701-1655	VR1, U16, U25, Q2, R8
10	701-1655	VR1, U17, U25, R8
11	702-1650	U17, Q3, R3, VR1, U2, Q1, CR1, CR2
	701-1655	U23, R1, Q15, Q17, RP8, RP3, RP4, RP2, Q4, CR6, U24, U11
12	702-1650	U17, Q3, R3, VR1, U2, Q1,CR1, CR2, VR3, U22, U5, U11, R2
	701-1655	U23, R1, Q15, Q17, RP8, RP3, RP4, RP2, Q4, CR6, U24, U11
13	701-1690	U17, U18, U11, Q22, Q25, Q2, CR19
	701-1655	U23, R1, RP8, Q16, RP3, Q14, RP4, RP2, Q12, U19, U24, CR9
14	701-1690	U15, U7, U12, Q21, U16
	701-0153	CR26, U2, CR22
15	701-1690	U16, U13, U7, U6, Q9
16	701-1655	U16, U14, U7, U3, Q3

Table 6-1 Troubleshooting Chart (continued)

TEST NO.	SUSPECT BOARDS	SUSPECT COMPONENTS
17	701-1655	U26, U17, U25, VR1
18	701-1655	U26, U16, U25, VR1, Q2
19	702-1650	U5, U22, U17, U11, Q3, U2, CR1, CR2, Q1, U16
	701-1655	U23, R1, RP8, Q15, RP3, Q17, RP4, RP2, Q4, CR6, U11, U24
20	701-1690	
	701-1655	
	701-0153	
21	701-0153	U10, DS1
	701-1655	U18
22	701-1690	U15, U7, U12, Q21, CR15, CR16, U16
	701-0153	CR26, U2, CR22
23	NO OPERATION	
24	701-1690	U16, U14, U7, U3, Q3, U9, U10, U11, Q24, Q25, Q19, CR14, Q16, CR4, CR3
	701-0153	C15, R19
25	701-1690	U16, U14, U7, U3, Q3, U9, U10, U11, Q24, Q25, U5, Q6, Q8, CR8, CR4, CR3
	701-0153	C15, R19
26	701-1690	U16, U14, U7, U3, Q3, U9, U10, U11, Q24, Q25, U5, Q13, CR9, Q4, Q10, Q12, Q5, Q7, CR4, CR3, CR18, Q20, U7
	701-0153	C15, R19
27	701-1690	U16, U13, U7, U6, Q9, CR10, CR11, Q2, CR19
	701-1655	U23, R1, Q16, RP3, Q17, RP4, RP2, Q8, CR9, U19, U24, R23
	701-0153	Q3, Q6, Q5, U3, Q4
28	701-1690	U16, U13, U7, U6, Q9, Q2, Q18, U17, Q11, CR2, Q14, U5
29	701-1690	U16, U15, U7, U12, Q21, CR15, CR16
	701-0153	CR26, U2, CR22
30	701-1690	U16, U14, U7, U3, Q3, CR4, CR3, U9, U10, U11, Q24, Q25, U5, Q6, Q8, CR8
	701-0153	C15, R19

Table 6-1 Troubleshooting Chart (continued)

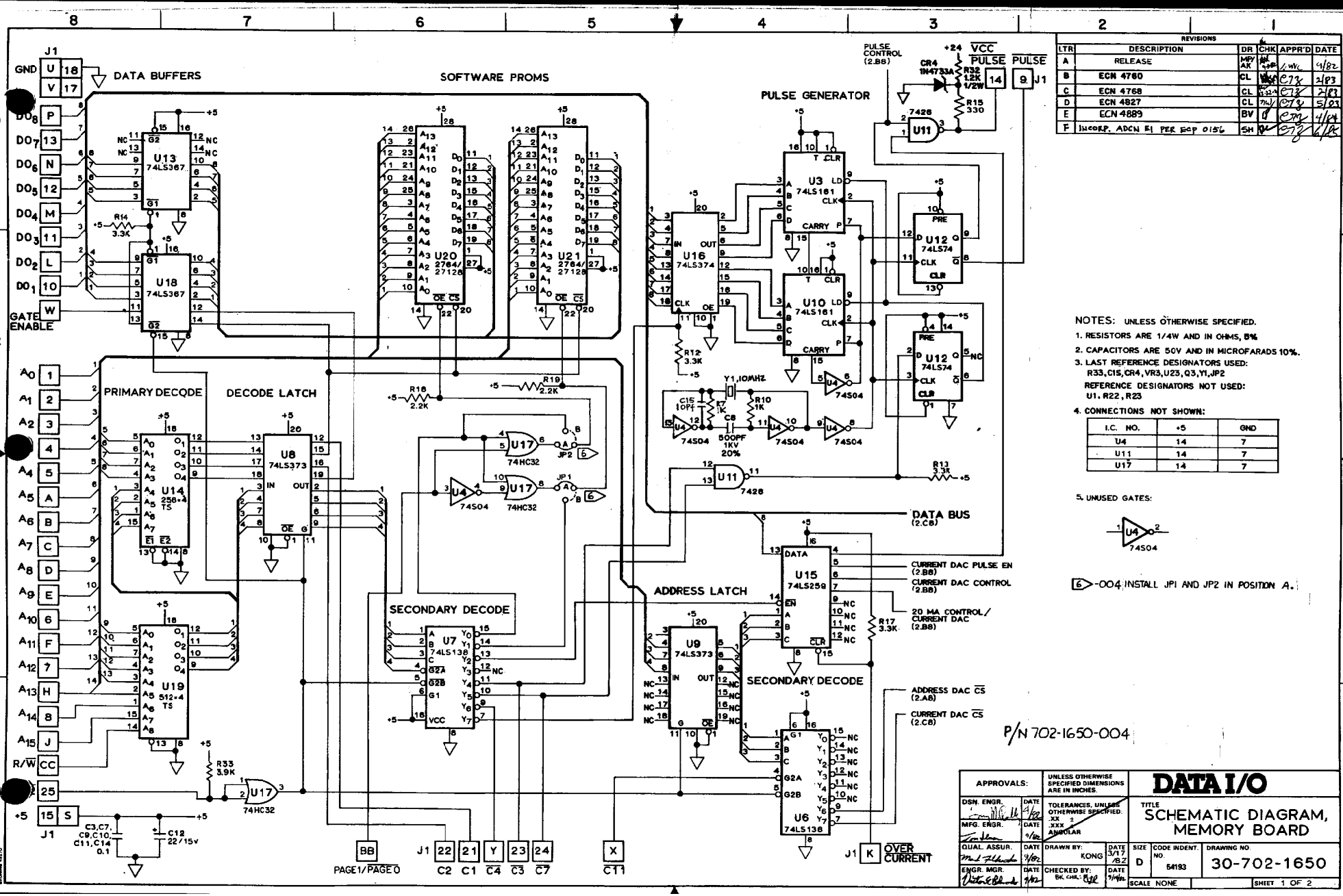
TEST NO.	SUSPECT BOARDS	SUSPECT COMPONENTS
31	702-1650	U23, U22, VR2, Q2, R28
	701-0153	CR19, Q1, U6
	701-1655	U4, U14, U20
32	701-1690	U18, U10, U5, U7, Q20, Q7, Q5, Q12, U9, CR9, Q13, U11, Q24
	701-0153	CR53, C15, R19
33	701-1690	U11, CR17, VR2, U18, Q19, Q16, U9, Q24, U10
	701-0153	CR54, R19, C15
34	701-1690	U16, U13, U7, U6, Q9, CR10, CR11
	701-0153	CR15, CR16, CR17, U3, CR18, Q6, CR46, C16, Q5, Q4
	702-1650	U5, VR3, U22, U17, U11, Q3, U2, Q1, CR1, CR2, VR1
	701-1655	U19, U24, U23, R1, Q16, RP3, Q17, RP4, RP2, Q8, CR9
35	702-1650	U5, VR3, U22, U17, U11, Q3, U2, Q1, CR1, CR2, VR1
	701-1655	U19, U24, U23, R1, Q16, RP3, Q17, RP4, RP2, Q8, CR9
36	701-1690	U16, U15, U7, U12, Q21, CR15, CR16
	701-0153	CR26, U2, CR22
37	701-1690	U16, U14, U7, U3, Q3, CR4, CR3, U9, U10, U11, Q24, Q25, U5, Q13, CR9, Q7, Q5, Q12, Q20, U7, CR18
	701-0153	C15, R19
38	701-1690	U16, U13, U7, U6, Q9, CR10, CR11
	701-0153	CR15, CR16, CR17, U3, CR18, Q6, CR44, C16, Q5, Q4
	702-1650	U5, VR3, U22, U17, U11, Q3, U2, Q1, CR1, VR1, CR2
	701-1655	U24, U11, U23, R1, RP8, Q15, RP3, Q17, RP4, RP2, Q4, CR9
39	701-1690	U16, U15, U7, U12, Q21, CR15, CR16
	701-0153	CR26, U2, CR22
40	701-1655	VR1, U16, U25, Q2, RP5, U28, U22, CR9, CR6, U24, U11, U19, CR4, CR7, R17
	701-0153	Q3, CR3, CR4, CR5, CR6, CR7, CR8, CR9, CR10, R17, CR44, CR46, CR57, CR59
41	701-1655	VR1, U16, U25, Q2, RP5, U28, U22, CR9, U24, U11, U19, CR4
	701-0153	Q3, CR3, CR4, CR5, CR6, CR7, CR8, CR9, CR10, R17, CR45, CR56, CR58, CR60
42	701-1655	VR1, U16, U25, Q2, RP5, U28, U22, CR9, U24, U11, U19, CR4
	701-0153	Q3, CR3, CR4, CR5, CR6, CR7, CR8, CR9, CR10, R17, CR45, CR56, CR58, CR60

Table 6-1 Troubleshooting Chart (continued)

TEST NO.	SUSPECT BOARDS	SUSPECT COMPONENTS
43	701-1655	VR1, U16, U25, Q2, RP5, U28, U22, CR9, CR6, U24, U11, U19, CR4, CR7, R17
	701-0153	Q3, CR3, CR4, CR5, CR6, CR7, CR8, CR9, CR10, R17, CR44, CR46, CR57, CR59
44	701-0153	U10
	701-1655	U18
	701-0154	DS1
45	701-1690	U16, U15, U7, U12, Q21, CR15, CR16
	701-0153	CR22, U2
	701-0154	CR12, C2
46	701-1655	U2, U3, U4, U14, U24, U16, U25, Q2
	702-1650	U23, U22, VR2, Q2
	701-0153	CR19, Q1, U6, U5, U4
	701-1690	Q7, Q5, Q12, U5, U9
47	701-1655	U2, U3, U4, U14, U24, U16, U25, Q2
	702-1650	U23, U24, VR2, Q2
	701-0153	CR19, Q1, U6, U5, U4
	701-1690	Q7, Q5, Q12, U5, U9
48	701-1655	U2, U3, U4, U14, U24, U16, U25, Q2
	702-1650	U23, U22, VR2, Q2
	701-0153	CR19, Q1, U6, U5, U4
	701-1690	Q7, Q5, Q12, U5, U9
49	701-1655	U2, U3, U4, U14, U24, U16, U25, Q2
	702-1650	U23, U22, VR2, Q2
	701-0153	CR19, Q1, U6, U5, U4
	701-1690	Q7, Q5, Q12, U5, U9
50	701-1655	Q4, Q8, Q12, Q5, Q14, Q15, Q16, Q17, U23, U24, U16, U25, Q2
	701-1690	U13, U7, U6, Q9, CR10, CR11, Q2, Q25, CR19
51	701-1655	Q6, Q11, Q9, Q7, Q14, Q15, Q16, Q17, U23, U24, U16, U25, Q2
	701-1690	U13, U7, U6, Q9, CR10, CR11, Q2, Q25, CR19
52	701-1655	Q4, Q8, Q12, Q5, Q14, Q15, Q16, Q17, U23, U24, U16, U25, Q2
	701-1690	U13, U7, U6, Q9, CR10, CR11, Q2, Q25, CR19
53	701-1655	Q6, Q11, Q9, Q7, Q14, Q15, Q16, Q17, U23, U24, U16, U25, Q2
	701-1690	U13, U7, U6, Q9, CR10, CR11, Q2, Q25, CR19

Table 6-1 Troubleshooting Chart (continued)

TEST NO.	SUSPECT BOARDS	SUSPECT COMPONENTS
54	701-0153	DS3, U10
	701-1655	U18
55	701-1690	U16, U15, U7, U12, Q21, CR15, CR16
	701-0153	CR27, U2, C18, CR22
56	701-0153	DS6, U10
	701-1655	U18
57	701-1690	U16, U15, U7, U12, Q21, CR15, CR16
	701-0153	U2, CR82, C25, CR22
58	701-0153	DS2, U10
	701-1655	U18
59	701-1690	U16, U15, U7, U12, Q21, CR15, CR16
	701-0153	U2, CR48, C13, CR22
60	701-0153	DS5, U10
	701-1655	U18
61	701-1690	U16, U15, U7, U12, Q21, CR15, CR16
	701-0153	U2, CR72, C23, CR22
62	701-0153	DS4, U10
	701-1655	U18
63	701-1690	U16, U15, U7, U12, Q21, CR15, CR16
	701-0153	U2, CR69, C20, CR22
64	701-0153	Q2, CR2, R11, R12, R13, R26, R27, R28, R29, R8, CR22, U2
	701-1655	U18, U22
65	701-1690	U16, U15, U7, U12, Q21, CR15, CR16
	701-1655	VR1, U16, U17, U25, Q2, Q3, Q1, R8
	701-0153	CR22, CR82, CR48, CR72, CR69, CR27, CR26, U2
	701-0154	CR12
66	701-1690	U16, U15, U7, U12, Q21, CR15, CR16
	701-1655	VR1, U16, U17, U25, Q2, Q3, Q1, R8
	701-0153	CR22, CR82, CR48, CR72, CR69, CR27, CR26, U2
	701-0154	CR12



REVISIONS					
LTR	DESCRIPTION	DR	CHK	APPR'D	DATE
A	RELEASE	MRY AK			9/82
B	ECN 4760	CL		C73	2/83
C	ECN 4768	CL		C73	2/83
D	ECN 4827	CL		C73	5/83
E	ECN 4889	BV		C73	4/84
F	INCORP. ADCN E1 PER ECP 0156	SH		C73	6/85

NOTES: UNLESS OTHERWISE SPECIFIED.

1. RESISTORS ARE 1/4W AND IN OHMS, 5%
2. CAPACITORS ARE 50V AND IN MICROFARADS 10%.
3. LAST REFERENCE DESIGNATORS USED:
   R33, C15, CR4, VR3, U23, Q3, Y1, JP2
   REFERENCE DESIGNATORS NOT USED:
   U1, R22, R23
4. CONNECTIONS NOT SHOWN:

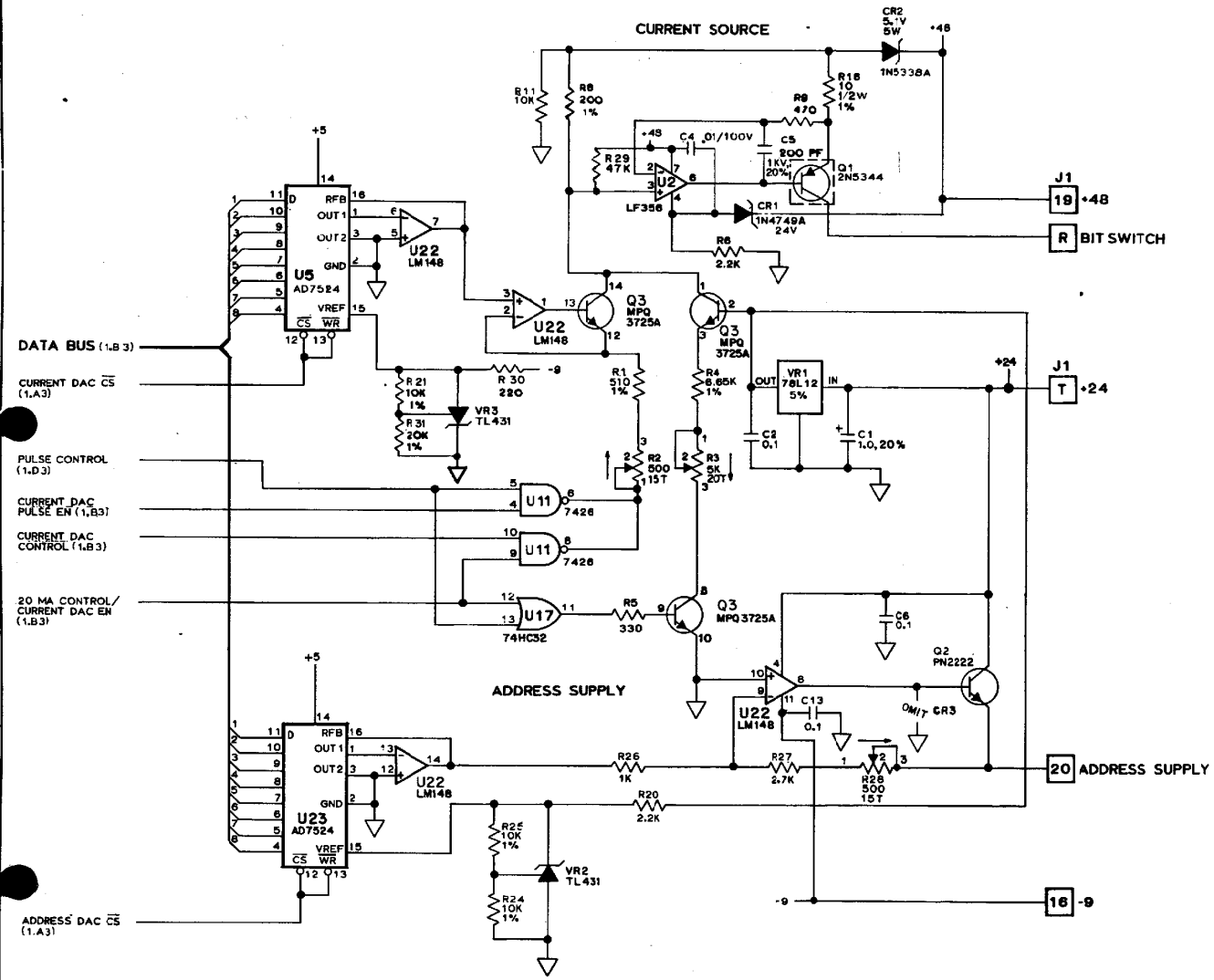
I.C. NO.	+5	GND
U4	14	7
U11	14	7
U17	14	7

5. UNUSED GATES:

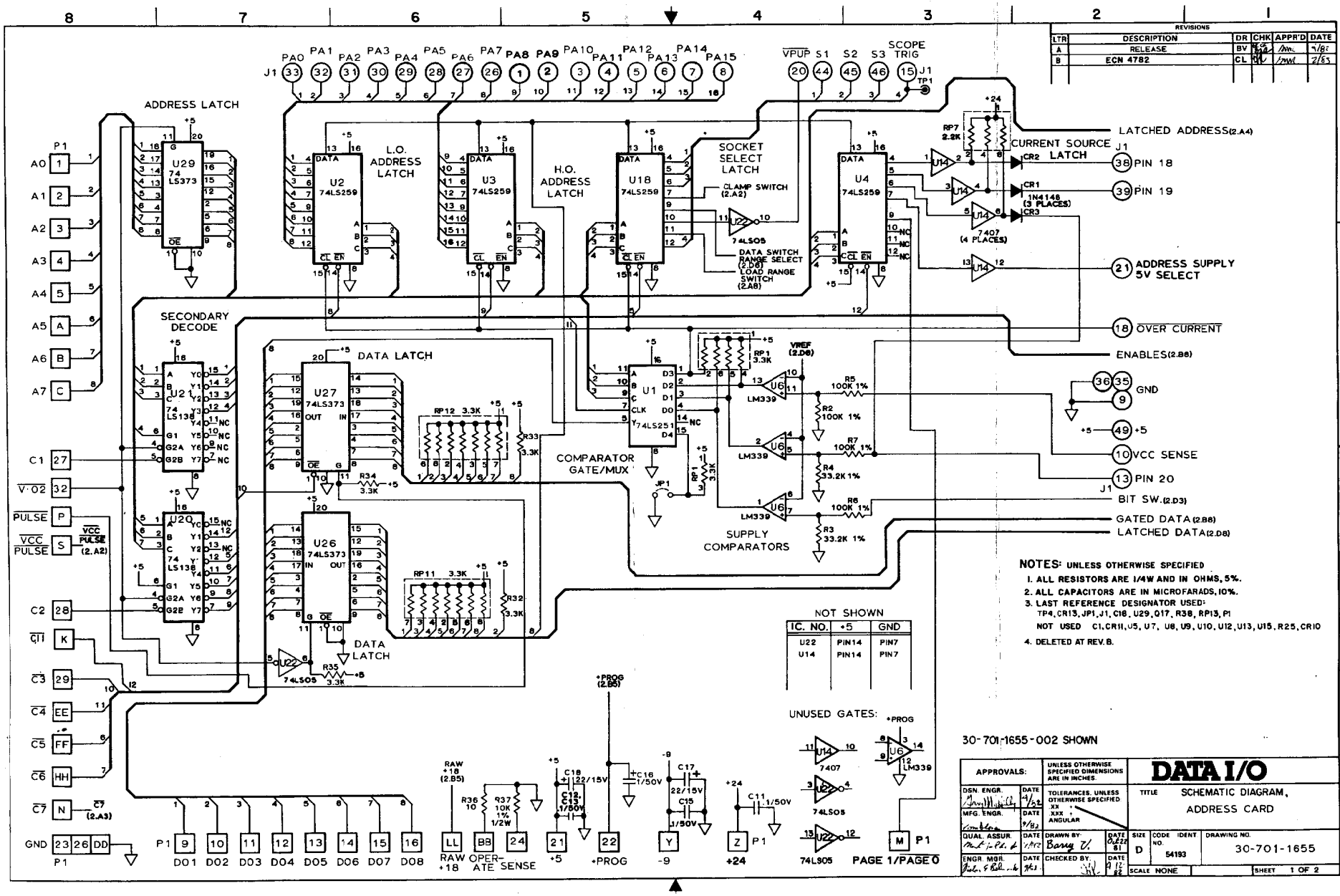
6 -004 INSTALL JP1 AND JP2 IN POSITION A.

APPROVALS:		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.	DATA I/O	
DSN. ENGR.	DATE 9/82	TOLERANCES, UNLESS OTHERWISE SPECIFIED: .XX ± .XXX ANGULAR	TITLE SCHEMATIC DIAGRAM, MEMORY BOARD	
MFG. ENGR.	DATE 9/82			
QUAL. ASSUR.	DATE 9/82	DRAWN BY: KONG	DATE 3/17/82	SIZE D
ENGR. MGR.	DATE 9/82	CHECKED BY: BK CHK:	DATE 9/1/82	CODE INDENT. NO. 54193
				DRAWING NO. 30-702-1650
				SCALE NONE
				SHEET 1 OF 2

REVISIONS					
LTR	DESCRIPTION	DR	CHK	APPR'D	DATE
F	SEE SHEET ONE				



APPROVALS:		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.	DATA I/O	
DSN. ENGR.	DATE	TOLERANCES, UNLESS OTHERWISE SPECIFIED: .XX ± .XXX ANGULAR	TITLE: SCHEMATIC DIAGRAM, MEMORY BOARD	
MFG. ENGR.	DATE			
QUAL. ASSUR.	DATE	DRAWN BY: KONG	DATE: 2/22/82	SIZE: D
ENGR. MGR.	DATE	CHECKED BY:	DATE:	CODE IDENT. NO.: 54193
		SCALE: NONE	SHEET 2 OF 2	DRAWING NO.: 30-702-1650



REVISIONS				
LTR	DESCRIPTION	DR	CHK	APPR'D	DATE
A	RELEASE	BV			1/82
B	ECN 4782	CL			2/83

NOTES: UNLESS OTHERWISE SPECIFIED

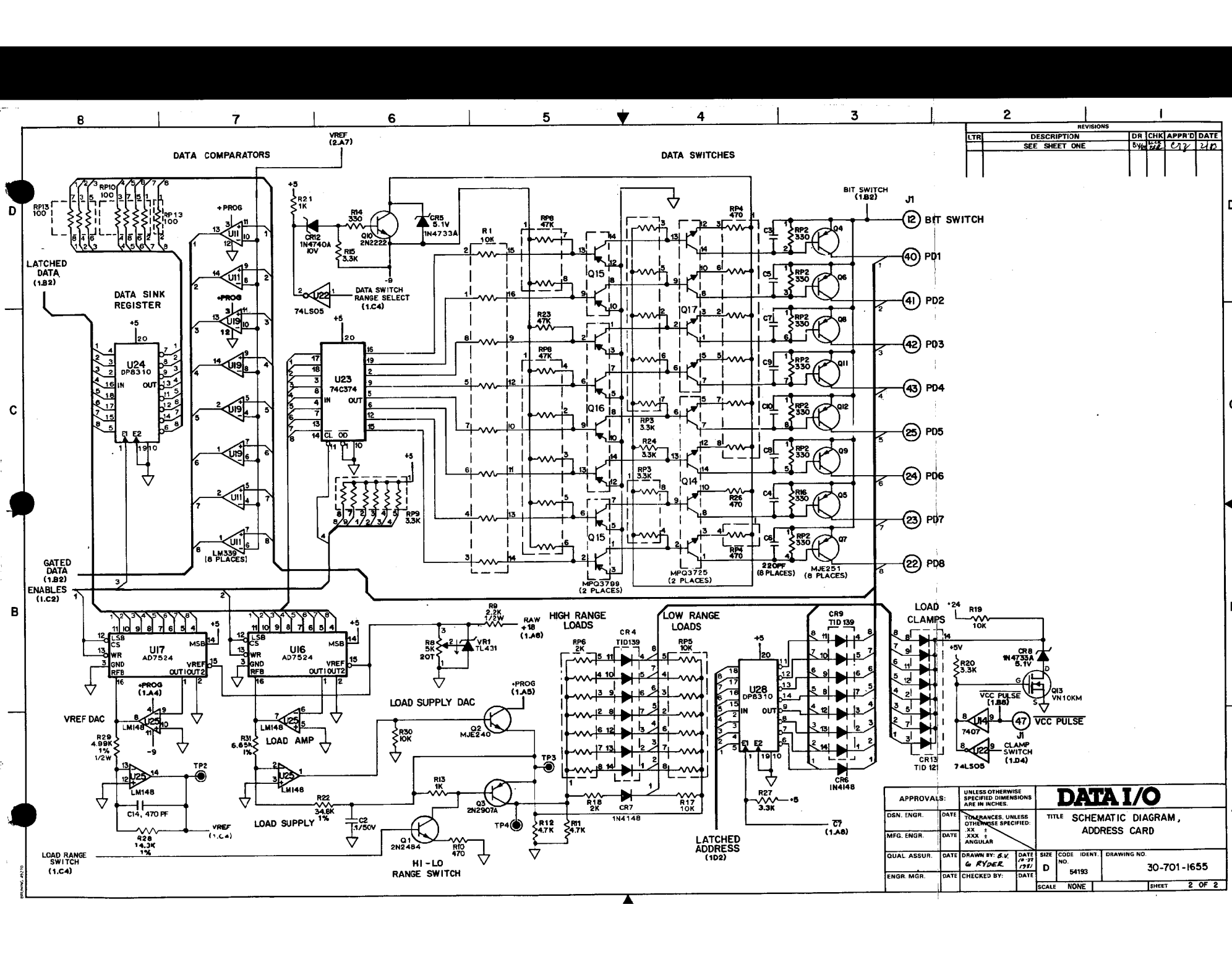
1. ALL RESISTORS ARE 1/4W AND IN OHMS, 5%.
2. ALL CAPACITORS ARE IN MICROFARADS, 10%.
3. LAST REFERENCE DESIGNATOR USED:
   TP4, CR13, JP1, J1, C18, U29, Q17, R38, RP13, P1
   NOT USED C1, CR11, U5, U7, U8, U9, U10, U12, U13, U15, R25, CR10
4. DELETED AT REV. B.

NOT SHOWN		
IC. NO.	+5	GND
U22	PIN14	PIN7
U14	PIN14	PIN7

30-701-1655-002 SHOWN

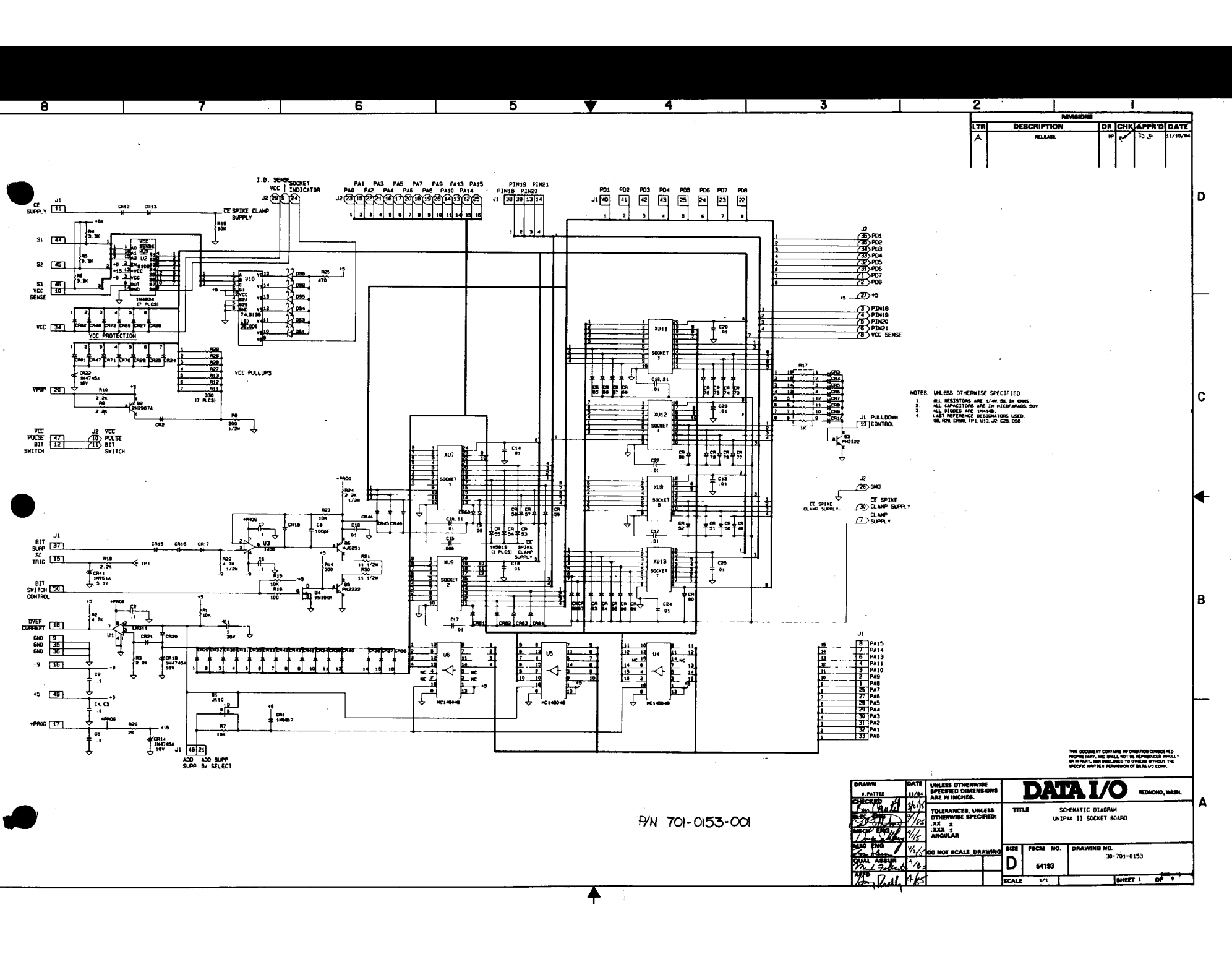
APPROVALS:		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.	DATA I/O	
DSN. ENGR.	DATE	TOLERANCES, UNLESS OTHERWISE SPECIFIED: XX ± .01, XXX ± .005, ANGULAR	TITLE	SCHEMATIC DIAGRAM, ADDRESS CARD
MFG. ENGR.	DATE			
QUAL. ASSUR.	DATE	DRAWN BY: Barry V.	DATE 04/22/81	SIZE D; CODE IDENT NO. 54193; DRAWING NO. 30-701-1655
ENGR. MGR.	DATE	CHECKED BY:	DATE	SCALE NONE; SHEET 1 OF 2

PAGE 1/PAGE 0



REVISIONS					
LTR	DESCRIPTION	DR	CHK	APPR'D	DATE
	SEE SHEET ONE	BV	WZ	CJZ	2/10

APPROVALS:		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.	DATA I/O	
DSN. ENGR.	DATE	TOLERANCES, UNLESS OTHERWISE SPECIFIED: .XX ± .XXX ± ANGULAR	TITLE SCHEMATIC DIAGRAM, ADDRESS CARD	
MFG. ENGR.	DATE			
QUAL. ASSUR.	DATE	DRAWN BY: B.V. G. RYDER	DATE 10-27-1981	SIZE D
ENGR. MGR.	DATE	CHECKED BY:	DATE	CODE IDENT. NO. 54193
				DRAWING NO. 30-701-1655
				SCALE NONE
				SHEET 2 OF 2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4
3
2
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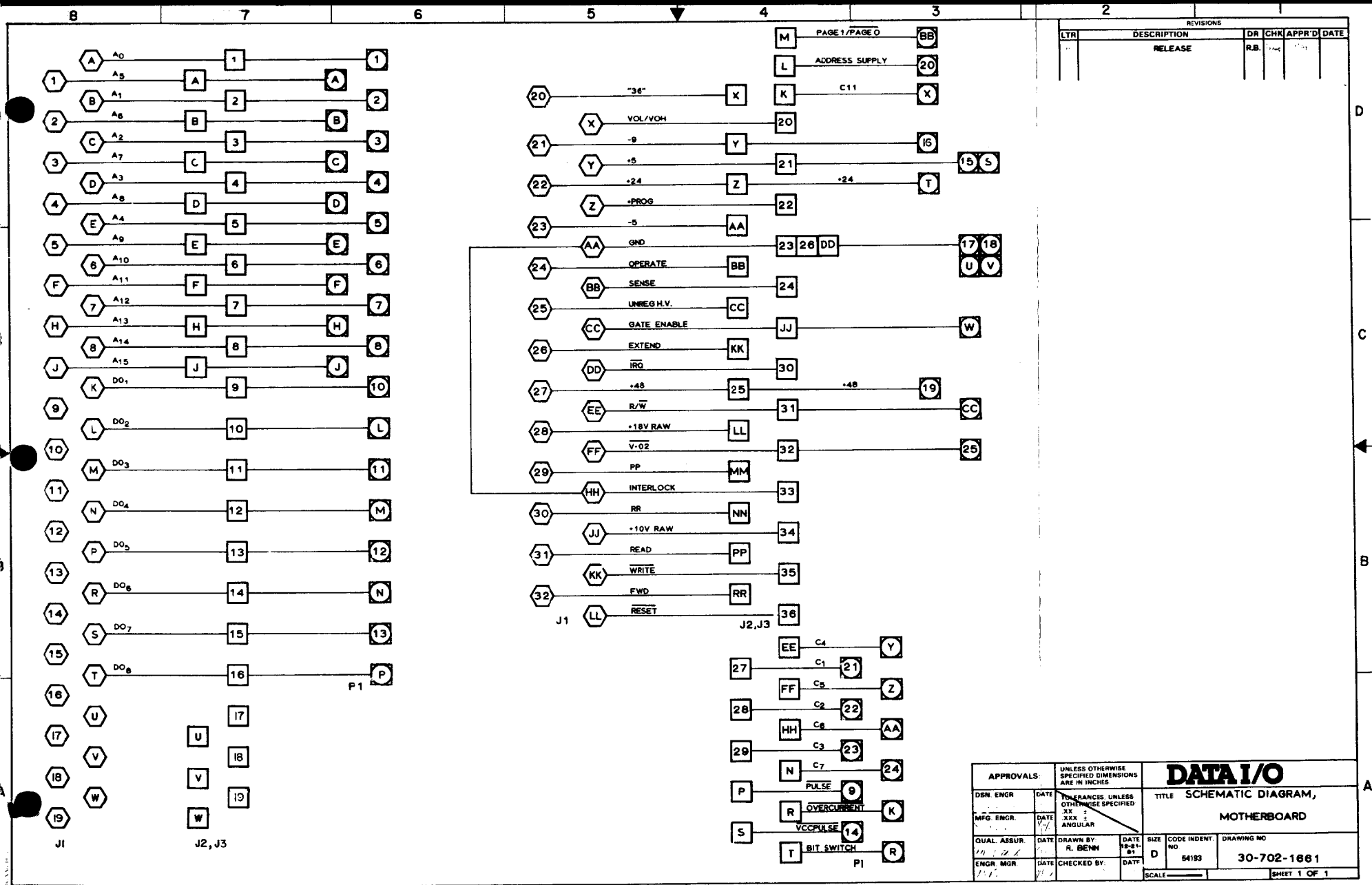
D
C
B
A
REVISIONS
LTR | DESCRIPTION | DR | CHK | APPR'D | DATE
A | RELEASE | MP | | | 11/15/84
I.D. SENSE SOCKET VCC INDICATOR
CE SPIKE CLAMP SUPPLY
VCC PROTECTION
VCC PULLUPS
PULLDOWN CONTROL
NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE 1/4W, 5%, IN OHMS
2. ALL CAPACITORS ARE IN MICROFARADS, 50V
3. ALL DIODES ARE 1N4148
4. LAST REFERENCE DESIGNATORS USED: Q5, R29, CR80, TP1, U13, J2, C25, DS6
ADD SUPP 5V SELECT
P/N 701-0153-001
DRAWN P. PATTEE 11/84
CHECKED
ENG
MFG ENG
QUAL ASSUR
APPD
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.
TOLERANCES, UNLESS OTHERWISE SPECIFIED: .XX ± .XXX ± ANGULAR
DO NOT SCALE DRAWING
DATA I/O REDMOND, WASH.
TITLE SCHEMATIC DIAGRAM UNIPAK II SOCKET BOARD
SIZE D FSCM NO. 54153 DRAWING NO. 30-701-0153
SCALE 1/1 SHEET 1 OF 9


8
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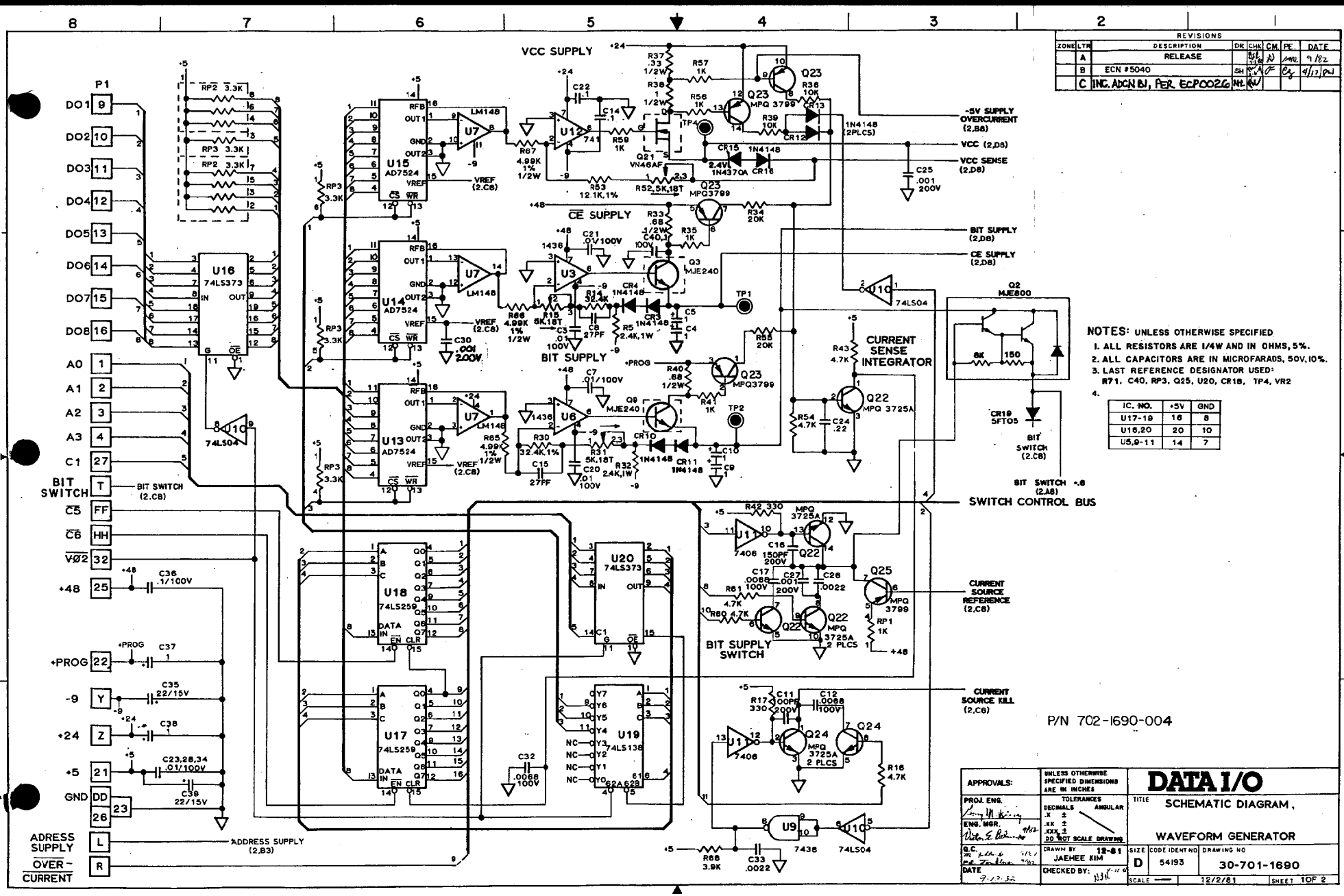
REVISIONS
LTR
DESCRIPTION
DR
CHK
APPR'D
DATE
RELEASE
R.B.
A0
A5
A1
A6
A2
A7
A3
A8
A4
A9
A10
A11
A12
A13
A14
A15
DO1
DO2
DO3
DO4
DO5
DO6
DO7
DO8
P1
J1
J2, J3
PAGE 1/PAGE 0
ADDRESS SUPPLY
"36"
C11
VOL/VOH
-9
+5
+24
+PROG
-5
GND
OPERATE
SENSE
UNREG H.V.
GATE ENABLE
EXTEND
IRQ
+48
R/W
+18V RAW
V-02
PP
INTERLOCK
RR
+10V RAW
READ
WRITE
FWD
RESET
C4
C1
C5
C2
C6
C3
C7
PULSE
OVERCURRENT
VCCPULSE
BIT SWITCH
APPROVALS
DSN. ENGR
MFG. ENGR.
QUAL. ASSUR.
ENGR. MGR
DATE
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES UNLESS OTHERWISE SPECIFIED
XX ±
XXX ±
ANGULAR
DRAWN BY
R. BENN
CHECKED BY
DATA I/O
TITLE
SCHEMATIC DIAGRAM,
MOTHERBOARD
SIZE
D
CODE INDENT. NO
54193
DRAWING NO
30-702-1661
SCALE
SHEET 1 OF 1



REVISIONS						
ZONE	LTR	DESCRIPTION	DR	CHK	CM.	PE.	DATE
	A	RELEASE					
	B	ECN #5040					
	C	INC. ADCN B), PER ECP0026					

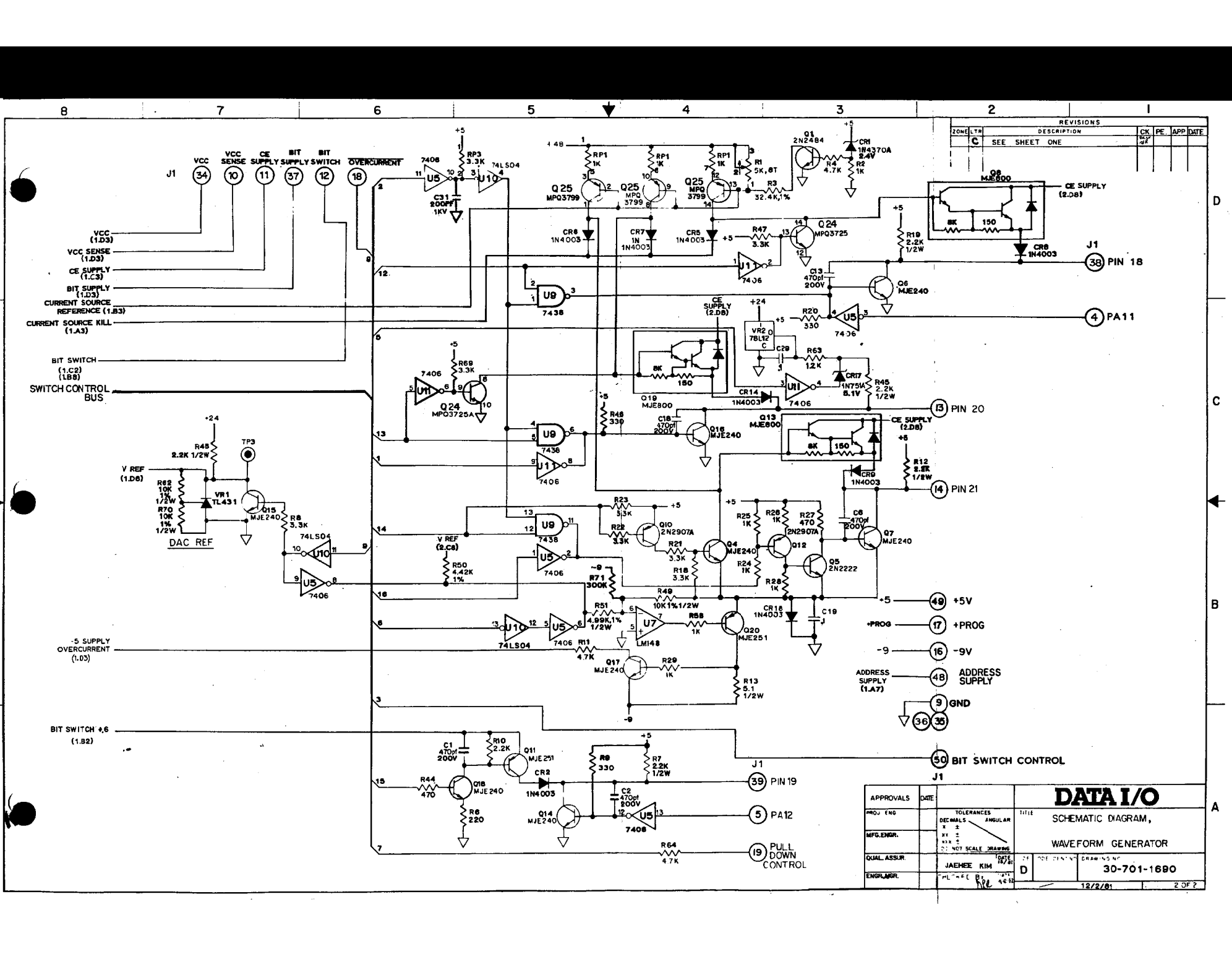
NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE 1/4W AND IN OHMS, 5%.
2. ALL CAPACITORS ARE IN MICROFARADS, 50V, 10%.
3. LAST REFERENCE DESIGNATOR USED: R71, C40, RP3, Q25, U20, CR18, TP4, VR2
4.

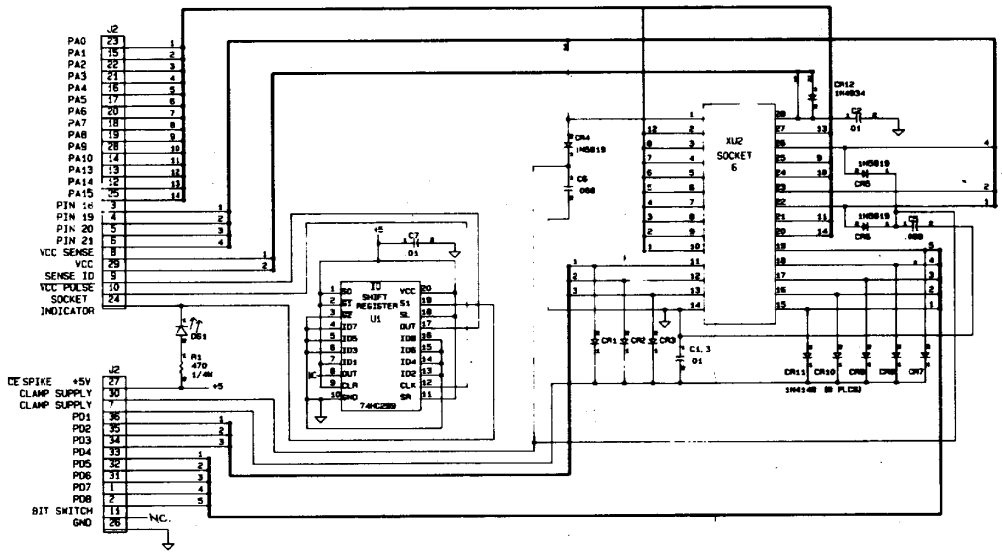
IC. NO.	+5V	GND
U17-19	16	8
U18,20	20	10
U5,9-11	14	7

P/N 702-1690-004

APPROVALS:	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	DATA I/O	
PROJ. ENG.	TOLERANCES DECIMALS .X ± .XX ± .XXX ± ANGULAR ± DO NOT SCALE DRAWING	TITLE	SCHEMATIC DIAGRAM, WAVEFORM GENERATOR
ENG. MGR. 4/82	DRAWN BY 12-81 JAEHEE KIM	SIZE D	CODE IDENT NO 54193
Q.C. 1/11/82	CHECKED BY:	DRAWING NO	30-701-1690
DATE 7-12-82	SCALE —	12/2/81	SHEET 1OF 2


REVISIONS
ZONE LTR DESCRIPTION CK PE APP DATE
C SEE SHEET ONE
J1
VCC (34)
VCC SENSE (10)
CE SUPPLY (11)
BIT SUPPLY (37)
BIT SWITCH (12)
OVERCURRENT (18)
VCC (1.D3)
VCC SENSE (1.D3)
CE SUPPLY (1.C3)
BIT SUPPLY (1.D3)
CURRENT SOURCE REFERENCE (1.B3)
CURRENT SOURCE KILL (1.A3)
BIT SWITCH (1.C2) (LB8)
SWITCH CONTROL BUS
-5 SUPPLY OVERCURRENT (1.D5)
BIT SWITCH *,6 (1.B2)
DAC REF
V REF (1.D6)
V REF (2.C6)
CE SUPPLY (2.D8)
PIN 18
PA11
PIN 20
PIN 21
+5V
+PROG
-9V
ADDRESS SUPPLY
GND
BIT SWITCH CONTROL
PIN 19
PA12
PULL DOWN CONTROL
APPROVALS DATE
PROJ. ENG
MFG. ENGR.
QUAL. ASSUR.
ENGR. MGR.
TOLERANCES
DECIMALS ANGULAR
DO NOT SCALE DRAWING
JAEHEE KIM
DATE 10/81
DATA I/O
TITLE
SCHEMATIC DIAGRAM,
WAVEFORM GENERATOR
SIZE D
DRAWING NO. 30-701-1690
12/2/81
2 OF 2

REVISIONS					
LTR	DESCRIPTION	DR	CHK	APPR'D	DATE
A	RELEASE	MP	[illegible]	DS	4/2/15



NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE 5% IN OHMS
2. ALL CAPACITORS ARE IN MICROFARADS

P/N 701-0154-001

DRAWN	DATE 3/05	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.	DATA I/O REDMOND, WASH.
CHECKED		TOLERANCES, UNLESS OTHERWISE SPECIFIED: .XX ± .XXX ± ANGULAR	TITLE SCHEMATIC DIAGRAM UNIPAK II PINOUT CARTRIDGE NO. 1
ENG	4/15	DO NOT SCALE DRAWING	SIZE C · FSCM NO. 54193 · DRAWING NO. 30-701-0154
MFG ENG	4/15		SCALE NONE · SHEET 1 OF 1
QUAL ASSUR	4/15		
APP'D	4/15		